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REALIZATION MODEL OF NON-VOLATILE SRAM USING MAGNETIC TUNNEL JUNCTION

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Abstract
In the last 10 years, FPGA circuits have developed rapidly, because of their flexibility, their ease of use and the low cost to design a function with them. However, the internal memories used in FPGA circuit could limit their future use. Most FPGA circuits use SRAM based flip-flop as internal memory. But since SRAM is volatile, both the configuration and information stored is lost. Internal Flash technology is sometime used to replace the external memory. However, it's slow re-programming and its limited number of writing cycles (up to 10^6) prevents its use to replace SRAM. By working at high writing and reading speed, MRAM (Magnetic RAM) technology is one of the best solutions to bring complete non-volatility to the FPGA technology while keeping the power dissipation low. An MRAM can be re-programmed 10^{12}times and has a large retention time up to 10 years. This technology is now mature and a lot of progress in its development has been done lately, especially by IBM, Freescale and Samsung [1].

Introduction
Normally the SRAM memory is volatile memory. Its store data during power is ON.When power is OFF,stored data is loss.The aim of this proposed model to change VOLATILE SRAM into NON-VOLATILE SRAM using MTJ(Magnetic Tunnel Junction).This Proposed design is designed by TANNER TOOL,Which is used to design Realization model of Non-Volatile SRAMbased on MTJ.The design of this model explain here.

Static random access memory
Static Random Access Memory is a type of semi-conductor memory where the word static indicates that, unlike DRAM it does not need to be periodically refreshed, as SRAM uses bi-stable latching circuitry to store each bit. SRAM inhibits data remanence but is still volatile in the conventional sense that data is eventually lost when the memory is not powered. Each bit in an SRAM is stored on four transistors that form two cross-coupled inverters. This storage cell has two stable states which are used to denote 0 and 1. Two additional access transistors serve to control the access to a storage cell during read and write operations. A typical SRAM uses six MOSFETs to store each memory bit.

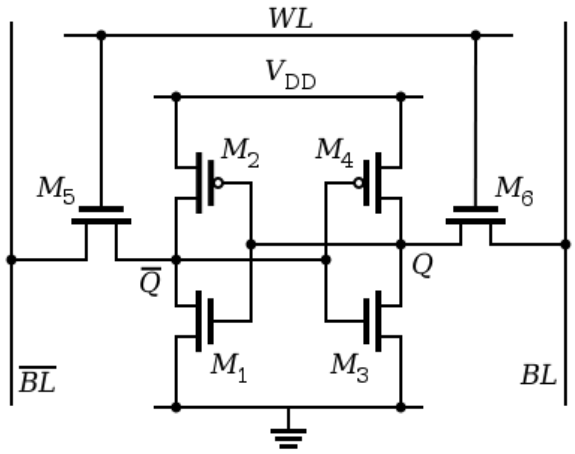

Figure 1:SRAM CELL

Access to the cell is enabled by the word line which controls the two access transistors M_5 and M_6which, in turn, control whether the cell should be connected to the bit lines: BL and $\overline{BL}$. They are used to transfer data for both read and write operations. Although it is not strictly necessary to have two bit lines, both the signal and its inverse are typically provided in order to improve noise margin. During read accesses, the bit lines are actively driven high and low by the inverters in the SRAM cell. This improves SRAM bandwidth compared to DRAMs. In a DRAM, the bit line is connected to storage capacitors and charge sharing causes the bitline to swing upwards or downwards.

The symmetric structure of SRAMs also allows for differential signalling, which makes small voltage swings more easily detectable. Another difference with DRAM that contributes to making SRAM faster is that commercial chips accept all address bits at a time. By comparison, commodity DRAMs have the address multiplexed in two halves, i.e. higher bits followed by lower bits, over the same package pins in order to keep their size and cost down. SRAM is used in personal computers, workstations, routers and peripheral equipment.

Sensing circuit in SRAM

A sense amplifier is an amplifier that senses the output on the bit lines and amplifies it. The sense amplifier that is used in the design is the 'Differential Voltage Sense Amplifier'. It takes small signal differential inputs (i.e. the bit line voltages), and amplifies them to a large-signal single-ended output. The differential approach presents numerous advantages over its single-ended counterpart. One of the advantages is the common mode rejection. It means that such an amplifier rejects noise that is equally injected in both the inputs.

The impact of those noise signals can be substantial, especially since the amplitude of the signal to be sensed is generally small. The effectiveness of a differential amplifier is characterized by its ability to reject the common noise and amplify the true difference between

the signals. The signals common to both inputs are suppressed at the output of the amplifier by a ratio called the common-mode-rejection-ratio (CMRR) [4].

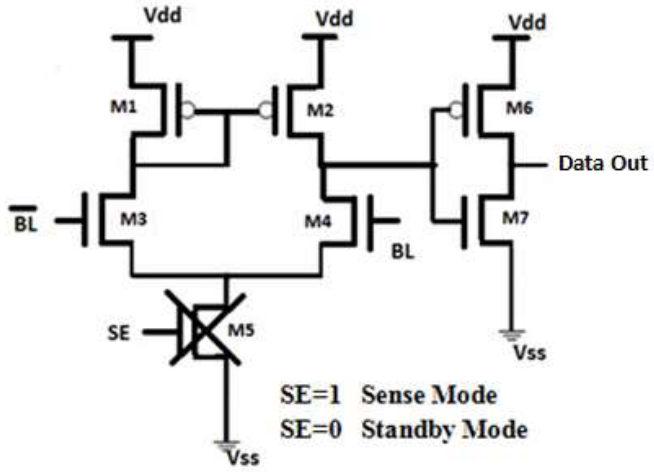

Figure2: Differential Sense Amplifier

Magnetic tunnel junction

MTJ uses differentiate between the two logic states. It contains two Ferro-magnetic layers which are separated from each other by a thin layer of insulator also known as barrier. The Ferro-magnetic layers are made up of Cobalt-Ferrous-Boron (CoFeBo). In Fig 3.2, Insulator layer or the barrier is made up of Magnesium-Oxide (MgO) is shown.

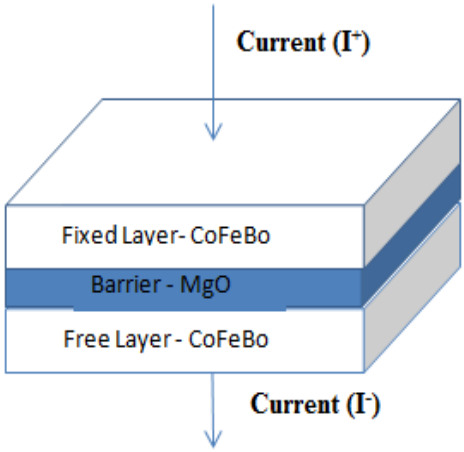

Figure3: Magnetic Tunnel Junction

Tunnel magneto resistance (TMR)

The ratio between the two resistances at zero bias is called as TMR ratio. Higher the TMR ratio, lower the resistance area.

$$TMR = \frac{R_{AP}-R_P}{R_P} \times 100\% \quad (1)$$

Where, R_{AP} is the electrical resistance in the anti-parallel state and R_P is the electrical resistance in the parallel state.

The fixed layer in MTJ is a permanent magnet whereas the free layer has Ferro-magnetic material that can be magnetised by passing a current (I) through it. Based on the field formed in the free layer the fields forms between the two layers. If both fields are in anti-parallel direction then high resistance is formed between the two layers .

Tunnelling

The fixed layer in MTJ is a permanent magnet whereas the free layer has Ferro-magnetic material that can be magnetised by passing a current (I) through it. Based on the field formed in the free layer the fields forms between the two layers. If both fields are in anti-parallel direction then high resistance is formed between the two layers [9].

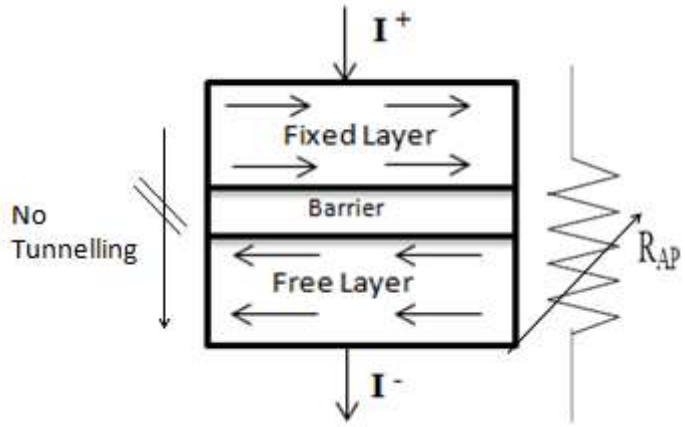

Fig 4.3 Anti-parallel field formed between the two layers.

Whereas when the fields formed between the two layers is parallel then low resistance is formed between the two layers and hence tunnelling occurs.

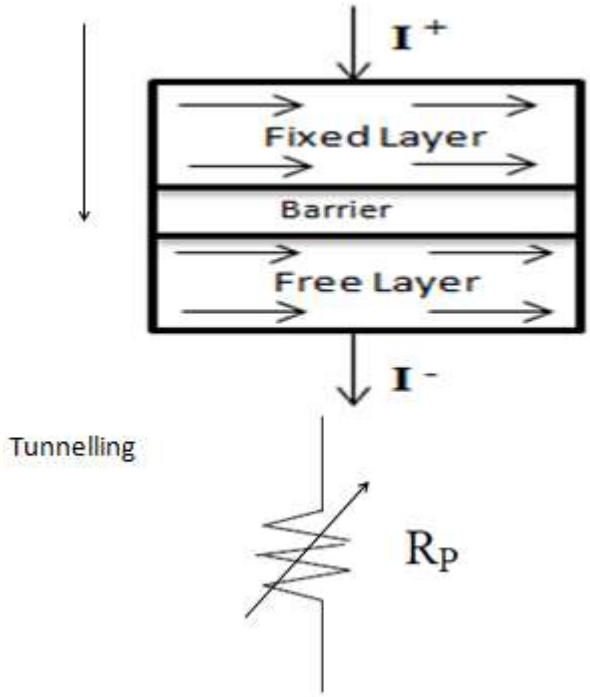

Fig 4.4 Parallel field formed between the two layers.

The two states of an MTJ can be formed by passing current. Fig 4.3explains about the anti-parallel field formed between the two layers whereasFig 4.4 explains about the parallel fields formed between the layers.

TMR ratio is used to determine the difference between the two resistances formed in the MTJ. Higher the difference between them, easier it will be to differentiate between the two resistances. The TMR decreases with both increasing temperature and increasing bias voltage [10].

Theoretical analysis of MTJ

Barrier conductance

Electron tunnelling through a thin insulating layer between two normal metal electrodes has been studied theoretically and experimentally for almost 40 years. Calculations based on rectangular and trapezoidal potential barriers using various approximations have shown that the tunnelling current should be directly proportional to the applied voltage for voltages very much lesser than the barrier height and should increase exponentially with voltage when the voltage becomes comparable to the barrier height [11].

We take a trapezoidal barrier shape and consider the two extreme cases of

- The WKB approximation.
- Perfectly sharp boundaries between metal and insulator.

Calculation of barrier conductance

Consider two metals a and b separated by an arbitrary potential barrier ϕ(x) [10]. Assuming the WKB approximation inside the barrier the tunnelling current density is given by

$$j = \frac{4\pi e}{\bar{h}} \Sigma \int_{-\infty}^{\infty} dE_{x\rho a}(E)_{\rho b}(E - eV)P(E_x) \times [f(E) - f(E - eV)] \quad (1)$$

where, $E_{\rho a}$and $E_{\rho b}$are the densities of states for a given transverse momentum and total energy E for system a and b respectively. The f (E) is the usual Fermi distribution function. E_x is the total energy in the direction perpendicular to the barrier. P (E_x) is the tunnelling probability which has the form.

$$P(E_x) = A \exp\left(-\frac{2}{\bar{h}} \int_0^d \{2m[\varphi(x`, V) - E_x]\}^{1/2} dx`\right) \quad (2)$$

where, d is the barrier thickness and $\varphi(x, V)$is the barrier height at the voltage V and the position x in the barrier. The pre-exponential factor A may depend on E_x.

Approximation used by simmons

The approximation used by the Simmons is to replace the barrier $\varphi(x, V)$by an average barrier $\bar{\varphi}(V)$ hence it is constant throughout the barrier and the tunnelling probability is simply reduced to

$$P(E_x) = A \exp\{(-(\frac{8m}{\bar{h}^2})^{1/2} \beta[\bar{\varphi}(V) - E_x]^{1/2} \int_d^0 dx^I\} \quad (3)$$

The correction factor β is assumed independent of E_x in order to perform the integration. By applying this

approximation all the information about barrier asymmetry is lost [12].

The tunnelling behaviour is usually modelled using the Simmons theory for tunnel junctions. The general equation for this theory is given below.

$$J = J_o\{\bar{\emptyset} \times \exp\left[-A\bar{\emptyset}^{\frac{1}{2}}\right] - (\bar{\emptyset} + eV) \times \exp\left[-A(\bar{\emptyset} + eV)^{\frac{1}{2}}\right] \quad (4)$$

Where, $J_o = \frac{e}{2\pi h(t_{ox})^2}$, $A = \left(\frac{4\pi t_{ox}}{h}\right)\sqrt{2m_e}$

Where 'e' is the charge of the electron, 'm_e' is the mass of the electron. '$\bar{\emptyset}$' is the potential barrier height which is found to be 0.4 for MgO. t_{ox} is the height of barrier in MTJ. 'h' is the Planck's constant which is 6.626×10^{-34}Js.

$$J = \frac{e}{2\pi h(t_{ox})^2}\{\bar{\emptyset} \exp\left[-\left(\frac{4\pi t_{ox}}{h}\right)\sqrt{2m_e}\bar{\emptyset}^{\frac{1}{2}}\right] - (\bar{\emptyset} + eV) \times \exp\left[-\left(\frac{4\pi t_{ox}}{h}\right)\sqrt{2m_e}(\bar{\emptyset} + eV)^{\frac{1}{2}}\right] \quad (5)$$

By ohm's law it's knownthat $V = R \times I$ (7)

Where V is the applied voltage, R is the resistance and I isthe Current flowing through it.

And Current Density $J = \frac{I}{A}$ (8)

Where A is the area of the cross section.
Now, the conductance physics model using the above equations, formed by Brinkman in 1970 is given below. It features the voltage bias dependence and is deeply influenced by the height of the barrier [13].

$$G(0) = \frac{3.16\times10^{10}\times\bar{\emptyset}^{\frac{1}{2}}}{t_{ox}} \times \exp[-1.025 \times t_{ox} \times \bar{\emptyset}^{\frac{1}{2}}] \quad (9)$$

$$\frac{G(v)}{G(0)} = 1 - \left\{\frac{A_0\times\Delta\emptyset}{16\times\bar{\emptyset}^{\frac{3}{2}}}\right\} eV + \left\{\frac{9}{128} \times \frac{A_0^2}{\bar{\emptyset}}\right\} (eV)^2 (10)$$

$$\text{where, } A_0 = \frac{4\times(2m_e)^{\frac{1}{2}}\times t_{ox}}{3\times\bar{h}} (11)$$

Here, $\Delta\emptyset = 0$ since barrier is symmetric.
The simplified resistance equations of the above equations (8) and (9) are given below which are used to express the resistance performance of an MTJ.

$$R(0) = \left\{\frac{t_{ox}}{223.76 \times \bar{\emptyset}^{\frac{1}{2}} \times \text{Surface}}\right\} \exp[1.025\times t_{ox}\times\bar{\emptyset}^{\frac{1}{2}}] \quad (12)$$

$$R(V) = \frac{R(0)}{1+\left[\frac{t_{ox}^2\times e^2\times m_e}{4\times\bar{h}^2\times\bar{\emptyset}}\right]\times V^2} (13)$$

R(0) is the higher value of resistance which is obtained due to the anti-parallel fields formed between the two ferromagnetic layers given by equation (12).
Whereas R(V) is the lower resistance value which is formed due to the tunnelling effect that occurs between the ferromagnetic layers through the insulating layer due to the parallel fields that are formed between the two ferromagnetic layers given by equation (13) [14].

Theoretical design of MTJ

In this design, an example of MTJ has been worked out and the two resistance values have been calculated by using simplified resistance equations (11) and (12). The diagram of the MTJ is given below.

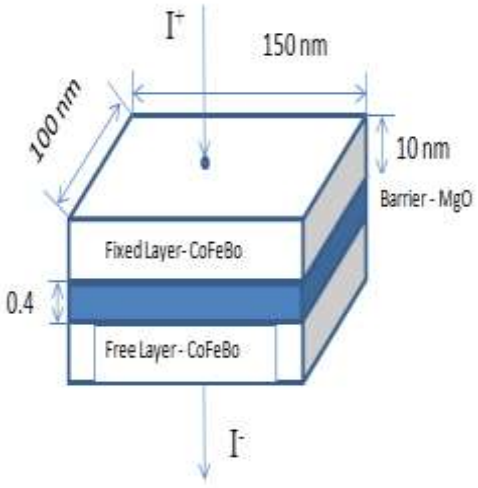

Figure 6: MTJ Design

For this model the following parameters have been considered,
Length of free layer = 150nm,
Width of free layer = 100nm,
Height of barrier = 100Å.

Surface area = (150×100) nm^2= $1.5\times10^{-14}m^2$
The two resistances calculated by putting the above values in equations (13) and (14) are obtained as,

R (0) = 1.415 KΩ
R (V) = 345.5 Ω

To calculate TMR ratio
TMR ratio is the difference between the two resistances formed in the MTJ. Resistance formed at the anti-parallel field is the higher resistance whereas the resistance formed at the parallel field is lower resistance. The higher the TMR ratio, lesser will be the resistance area (R_A) [15]. And hence it will be easier to differentiate between the two logic states. Hence the higher TMR ratio is desirable.
From equation (1),

$$TMR = \frac{R_{AP} - R_P}{R_P} \times 100\%$$

TMR = 309.55%

Here a high TMR ratio is obtained which is desirable. Hence it becomes easy to differentiate between the two resistances.

Non-volatile SRAM based on MTJ
Realization Design by Tanner Tool

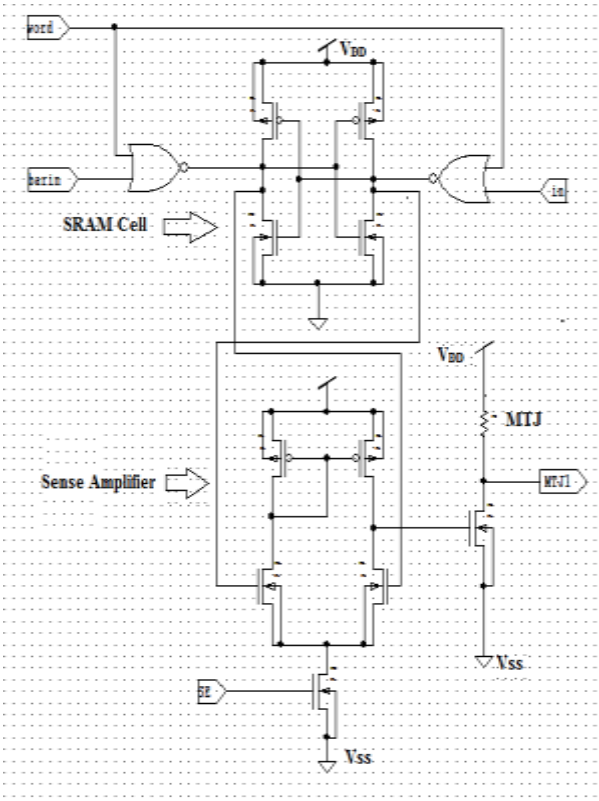

Figure 7: Non-volatile SRAM based on MTJ

Four BIT non-volatile SRAM using MTJ

A four-bit Non-Volatile SRAM is designed using Tanner Tool (0.25µm) technology. The circuit diagram of Non-Volatile SRAM cell is given in Fig-7 .This figure contains four SRAM cells each connected to an MTJ. The inputs are given to the SRAM cells from where it is fed into the sense amplifier.

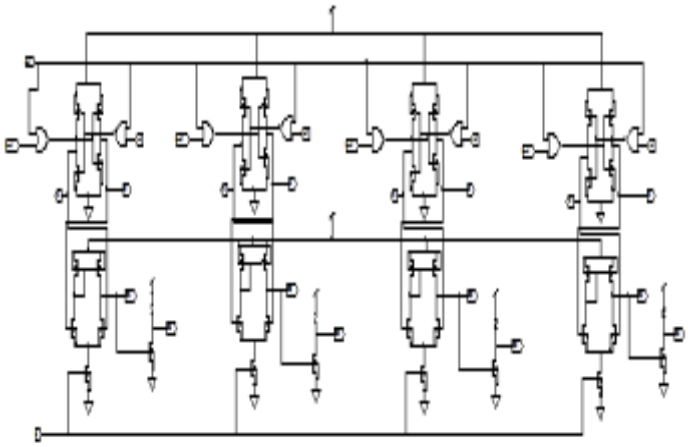

Figure 8: Four bit non-volatile SRAM.

The output of the sense amplifier is fed into the MTJ. The detailed diagram of a single cell of SRAM is given in Fig-1. The data is given to the SRAM cell in which it is stored. The output of SRAM is taken with the help of differential sense amplifier. Its output is then fed into the MTJ.

The waveforms of the output of SRAM cell, MTJ output is taken by simulating it in Tanner Tools. The input to the SRAM cell is given as 0110 as shown in Fig 9. and is fed into the sense amplifier. The output of the sense amplifier is given in Fig 10. The output of MTJ is taken as logic '0' when its output voltage is less than 90mV and it is taken as logic '1' when it is more than 200mV.

The following graphs are obtained from the simulation of the SRAM cell with the MTJ realization. The input 0110 given to the SRAM cell as shown in Fig 9.

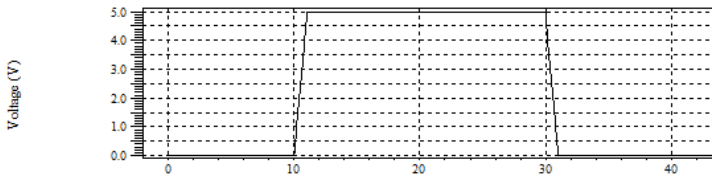

Figure9: Input to SRAM cell (0110)

The output of the SRAM cell is given to the sense amplifier which cancels the common noise and amplifies the difference between the two signals.

The output of the sense amplifier is then fed to the input of the realized MTJ. This MTJ stores the result. The output of the MTJ is given in Fig 10. The output voltage range that is obtained in this circuit is from 90mV to 220mV. The output logic takes it as logic '0' when the output of MTJ is less than 90mV and it takes it as logic '1' when its output is greater than 200mV.

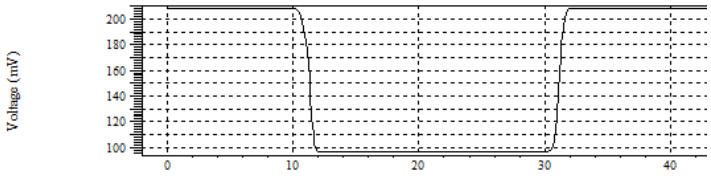

Figure 10: Output voltage across MTJ

The two distinct resistances are found using the tanner tool simulation. The higher resistance which denotes the resistance formed due to the parallel field formed between the two layers is found to be 1.2kΩ and the lower resistance that is formed due to the parallel field formed between the two layers is found to be of 260Ω as shown in Fig 11.

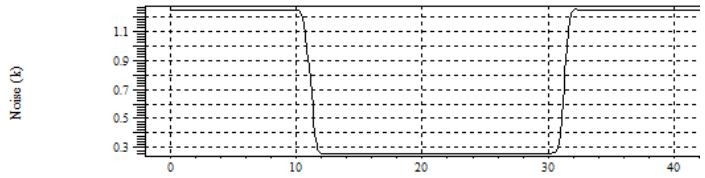

Figure 11: Resistance of MTJ

Drain current through the MTJ is also found out from the simulation. It is given in Fig 12. The range of current is found to be 160µA to 360µA.

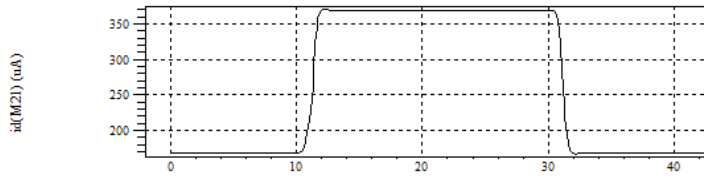

Figure 12: Drain current at MTJ

The power consumption of the MTJ is also calculated using tanner simulation. It is found to be 50µW for higher resistance whereas it is 110µW for the lower resistance. It is shown in Fig 13.

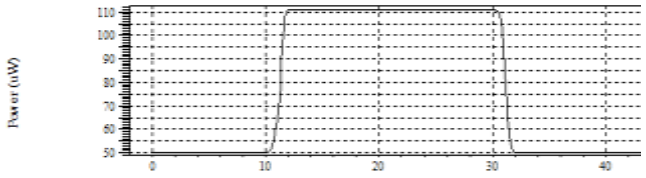

Figure 13: Power consumption of MTJ

TABLE I: Result of NV-SRAM at differ.,input bit

Input Bits	Output Voltage (mV)		Drain Current (μA)		Resistances (Ω)		TMR ratio (%)	Power (μW)	
	Logic '0'	Logic '1'	Logic '0'	Logic '1'	Logic '0'	Logic '1'		Logic '0'	Logic '1'
1010	210	90	160	360	1200	260	314.45	50	110
1001	210	90	160	360	1200	260	314.45	50	110
0110	210	90	160	360	1200	260	314.45	50	110
1110	210	90	160	360	1200	260	314.45	50	110
1011	210	90	160	360	1200	260	314.45	50	110

Hence the higher value of resistance which is the anti-parallel field resistance of MTJ is found to be 1.2KΩ and the parallel field resistance is obtained as 260Ω. And the power consumption of MTJ is found to be as low as 50μW for higher resistance and 110μW for lower resistance.

Conclusion

Most FPGA circuits use SRAM based flip-flop as internal memory. But since SRAM is volatile, both the configuration and information stored is lost. Hence a Non-volatile SRAM is designed using a Magnetic Tunnel Junction and is simulated in the Tanner Tools. The two resistances are calculated and are found to be1.2kΩ for logic '0' and 260Ω for logic '1'. The currents flowing through the MTJ during the two states are easily differentiable. At logic '0', 120μA current flows whereas at logic '1',0.3mA current flows. Thus the maximum current flow is as low as 360μA which is very low.The TMR ratio of 314.45% is obtained. The more the TMR ratio, the more will be the resistance area in the MTJ,hence it is easy to differentiate between the two logic states at the output of MTJ. The power consumption of the Non-Volatile SRAM differentiate between the two logic states at the output of MTJ. The power consumption of the Non-Volatile SRAM is found to be 50μW for higher resistance and 110μW for the lower resistance. Hence the SRAM cell which has been designed and realized using MTJ is a non-volatile device and can be used to store the data from the output of the SRAM cell as tabulated in Table I

The application of full adder has been done and the two outputs (SUM and CARRY) are stored in two MTJs. The drain current flowing through it is found and the two resistances are obtained as shown in Table I. The drain current flowing through the MTJ is obtained as 100μA for logic '0' and 270μA for logic '1' and the voltage obtained across the MTJ is 95mV for logic '1' and 550mV for logic '0'. The two resistances obtained are $R_H(0)$ for logic '0' and $R_L(1)$ for logic '1'. Where $R_H(0)$ is 5.5kΩ and $R_L(1)$ is 330Ω. The input voltage supplied to the MTJ is 0.8 volts.

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