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PERFORMANCE ANALYSIS OF HIGH SPEED CMOS FULL ADDER CIRCUIT FOR LOW VOLTAGE VLSI CIRCUIT DESIGN IN NANOMETER

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Abstract
As the technology scaling reduces the gate oxide thickness and the gate length thereby increasing the transistor density and also reduces the delay. Reduced gate lengths result in an increase in the leakage power dissipation.. Power optimization is also important for many designs to minimize package cost and maximize battery back-up of system. Power optimization is possible at each level of design process from higher architecture level to lower physical level. In this paper we have compared some existing Adder circuit designs for power consumption, delay, PDP at different frequencies viz 10 MHz, 200 MHz and 1 GHz. Simulations are performed by using Cadence Virtuoso at 180nm CMOS technology and the simulation results are analyzed to verify the existing designs. Maximum saving of power is at low frequency by Hybrid GDI adder circuit is 96.3% with respect to C-CMOS and significant improvement is observed at other frequencies also. Hybrid GDI needs less number of transistors as compared to standard CMOS technique. Need of less transistors leads to low cost of device.

Introduction
Today, electronic devices play a very important role in every one's day to day life. Devices such as mobile phone, ipad, laptop, pocket calculator become necessity to live a comfortable life. Consumer prefers portable and battery powered electronic devices. Earlier in 1990's, performance and speed was the important parameters to design any system but now with the growing trend towards portable computing and wireless communication, power dissipation has become one of the most critical factor in the continued development of microelectronics technology [1].

In very large scale integration circuit power consumption play important role in CMOS circuit. In a CMOS circuit there are mainly two types of power consumption static and dynamic power consumption. Static power consumption is due to leakage current and dynamic power consumption is due to charging and discharging of capacitor and third power consumption is due to short circuit. For the decade getting high performance, high packing density and low power reducing the transistor size scaling is required. Using such type of methodology the leakage power of transistor has increase exponentially. In CMOS circuit reduction of threshold voltage due to voltage scaling leads to increase in sub-threshold leakage current and hence static power dissipation. When the technology is scaled supply and threshold voltage also scaled. Due to reducing transistor size, the channel length also become short which increase the leakage current through a transistor in off condition. Leakage power is a very serious problem in mobile application so resolving this, different type of technique are used at circuit level and process level.

Recently, the GDI (Gate Diffusion Input) technique is emerged as a promising alternative to Standard CMOS Logic [4]. GDI full adders are followed by inverters to improve the performances with respect to conventional single full adder chain. The propagation delay, dynamic and leakage power dissipation can be optimized by changing the number of full adders between two consecutive inverters. HSPICE simulation using TSMC 0.35µm and 0.18µm CMOS technologies evaluated propagation delay and average power for minimum power design. Their proposed circuit is 18 to 48% and 7 to 26% faster than the previous circuits at 0.35µm and 0.18µm CMOS technologies respectively. In this research, different circuit style and methodologies are analyzed. Several circuit design techniques are compared in order to find their efficiency in terms of speed and power dissipation [6,7]. Each one has its own merits and demerits. Conventional static CMOS has been a technique of choice in most digital design. Alternatively, Pass Transistor Logic has been suggested for low power, high speed systems. The adder based on GDI technique consist of a regular structure repeatedly using a gdi cell for implementing various circuits within the adder the main disadvantage of the gdi adder is loss of voltage swing which reduces the driving capability of the adder[8-9].

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The floating adder [10] is another low power high speed full adder circuit which works well at high frequencies. its low power characteristics and performance stability at frequencies as high as 1Ghz are of great advantage at such high speeds. the disadvantage of the floating adder is that it produces weak '0' and '1' at sum and carry output respectively.
Another technique of adder design utilizes the advantage of multiple techniques while designing the adder circuit, this hybrid technique provides one the liberty to gather the advantages of various techniques within one circuit various hybrid designs have been proposed over the years. A high speed low power variant is been discussed here. This hybrid adder has low power high speed full swing output with good driving capability[11],[12].

Paper is organization as follows: The section II, describes previous work which consist various types of Adder circuit. Section III, presents Simulation and result discussion by using Cadence virtuoso EDA tool. Finally the conclusion is presented in section IV.

Previous Work

The CMOS full adder consists of 28 transistors with regular CMOS structure [7] (pull-up and pull-down networks) as shown in Fig. 1. The CMOS full adder provides full voltage swing. One of its main merits is its robustness against voltage scaling and transistor sizing. The complementary design leads to very simple circuit of a full adder. The main drawback of the adder is the use of large number of PMOS transistors in its design due to which its input capacitance is very large also large area is required for the circuit due to these PMOS transistors[8].

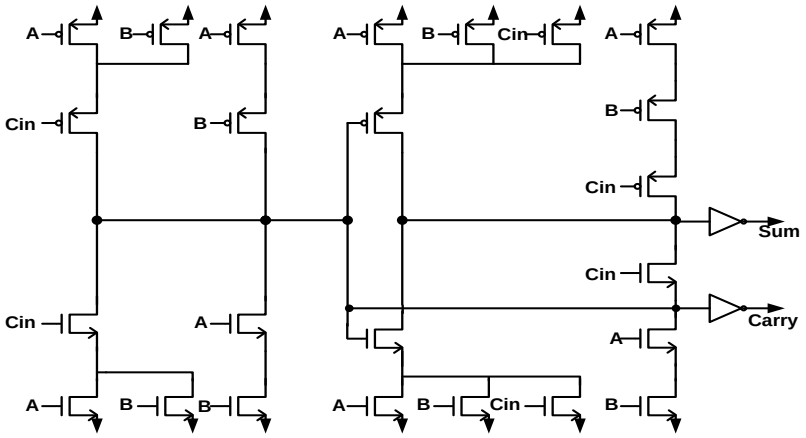

Figure.1. Circuit structure for complementary CMOS (C-CMOS)

Complementary Pass Transistor Logic (Cpl)
The complementary pass transistor logic based full adder [7],[15] consists of 32 transistors in a dual rail structure as shown in the figure. This full adder circuit provides full voltage swing output and good driving capability due to the static output inverters as shown in Figure.1. The fast differential stage of cross coupled PMOS transistors enables high speed operation. The main disadvantage of the CPL full adder circuit is large power consumption due the increased number of internal nodes and static inverters which increase the leakage and static power dissipation.

Gdi Adder
The Gate Diffusion Input technique (GDI) provides the implementation of different complex functions using only two transistors. Compared to CMOS and existing PTL techniques, the GDI technique is suitable for design of fast and low power circuits using reduced number of transistors. The GDI method [4, 5] is based on the use of simple cell which looks exactly like the basic inverter. The detail methodology of GDI is explained in next chapter. Here we explained few research findings about GDI technique as shown in Figure.2 (a).

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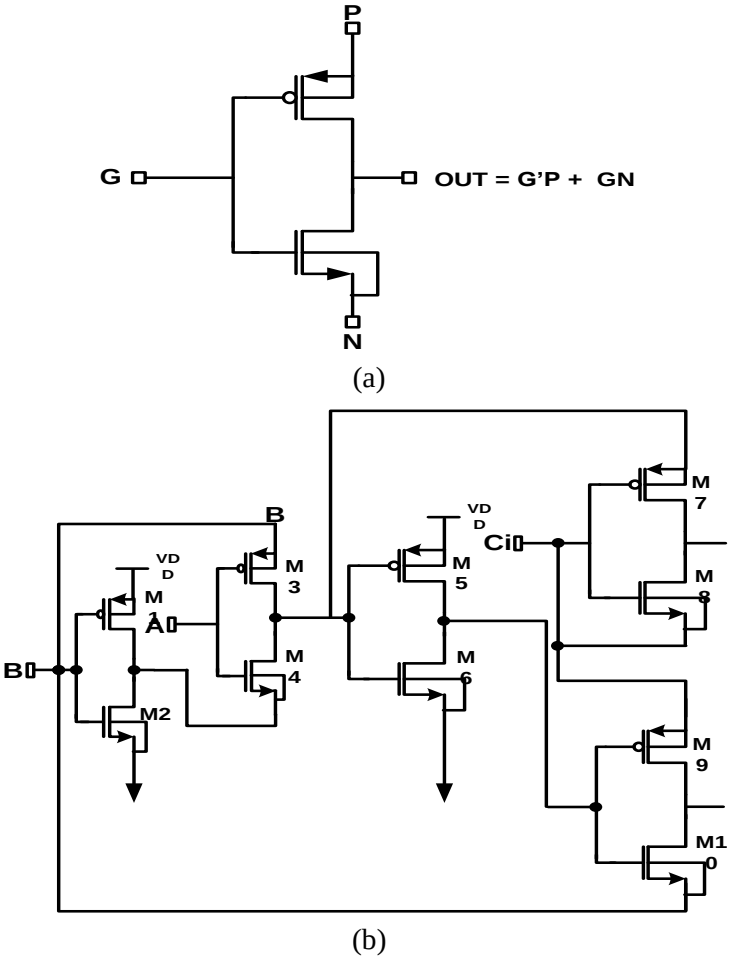

Figure.2: (a). Basic GDI cell (b). 10 Transistor design of a GDI based adder

As the figure shows the standard cell resembles to the inverter except that it has three inputs and the bulks of both PMOS and NMOS transistors are connected to p and n respectively the cell is being fabricated using twin well CMOS or silicon on insulator (SOI) technologies[9]. The GDI cell is capable of carrying out various logic function based on various input configurations[8]. The use of GDI cell reduces the number of transistors required for designing the adder circuit to great extent which results In a reduction in power dissipation and area required for the circuit. a 10 transistor design of a full adder using GDI technique[16] is shown in the fig. 2 (b)

Floating Full Adder

This adder utilizes 8 transistors for the design of an adder circuit if both input and its complements are available and uses 12 transistors if complement of the inputs is not available. The structure of a floating adder is shown in Fig. 3.

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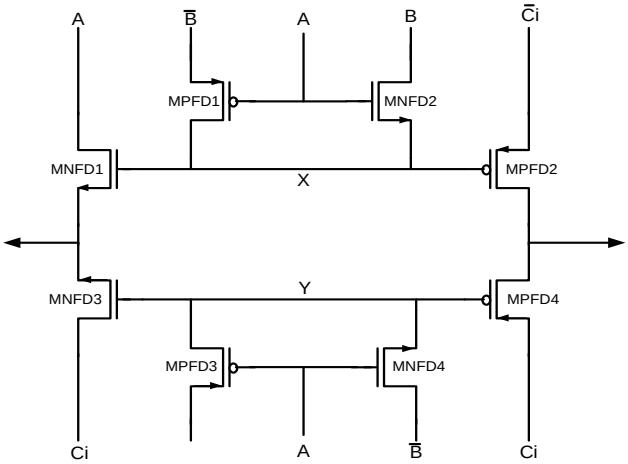
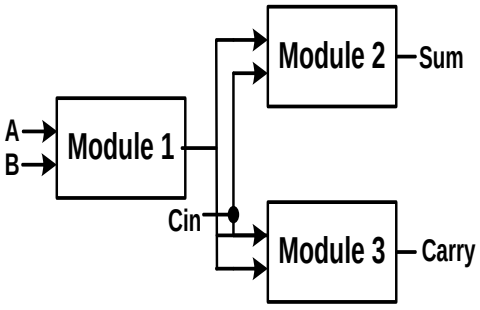


Figure.3: Structure of a floating adder

As can be seen from the figure, two of the internal nodes (X and Y) are not directly connected to any of the inputs, hence called floating adder. Power in the circuit is reduced due to the reduced switching activity in the circuit. The adder proves to be a promising design for high speed and low power circuit design and have good performance stability against high frequency. The main drawback of the circuit is the degradation of output voltage levels due to the inability of pmos and nmos transistors to pass 0 and 1 respectively. the weak '0' and '1' at the sum and carry out put respectively lead to poor driving capability but this can be sorted out using buffers at the output stages[10].

Hybrid Adder

The hybrid logic style exploits the advantages of different logic styles to get the desired performance from an adder. In hybrid logic style the full adder is divided into different modules as shown in Figure 4(a) and different design styles are used to optimize each module[8],[11],[12].



(a)

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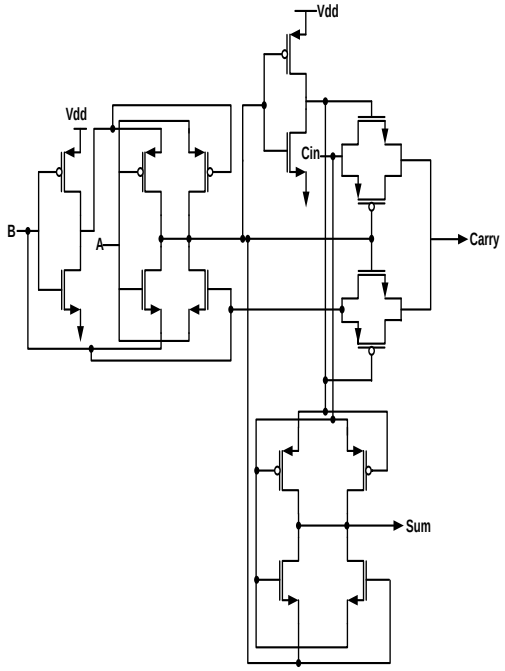

(b)

Figure.4: (a) hybrid design methodology (b) 16 transistor hybrid adder

Module 1 generates XOR and XNOR functions of inputs A and B, as intermediate outputs module 2 and module 3 consist of the circuitry that utilizes these intermediate signals along with Cin signal to generate the sum and carry outputs[13].

A 16 transistor hybrid adder[14] is shown in figure 4 (b). The above hybrid adder gives full swing output at high frequencies and satisfactory performance stability performance stability at high speeds. This adder utilizes 16 transistors however we can reduce it to get reduced area and power of the circuit[14].

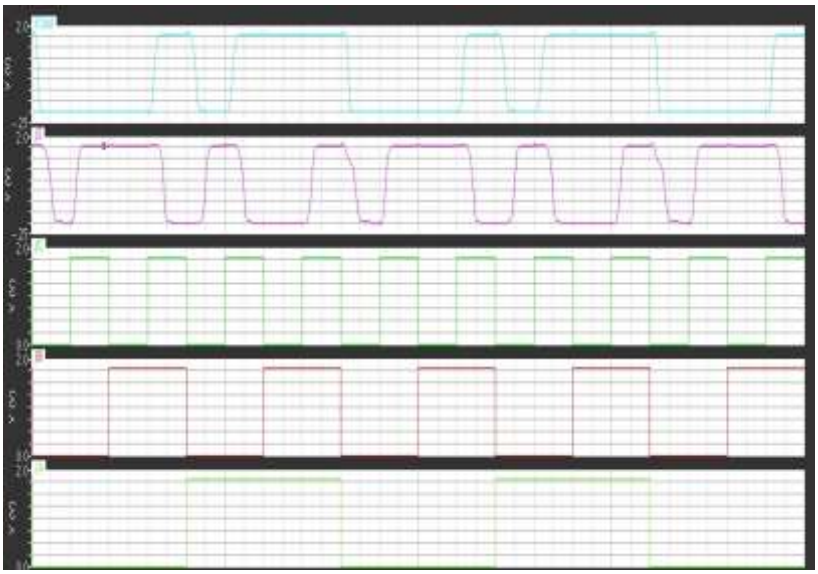

Figure.5: Output Waveform of Hybrid Adder Circuit

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Simulation and Result Discussion

All the existing and proposed circuit is simulated in Cadence Virtuoso at 180nm technology with supply voltage of 1.8V. Power consumption is calculated with the variation of frequency at lower frequency (10MHz), middle frequency (200MHz) and high frequency (1GHz). We observe that as we increase the frequency the power consumption of the adder circuit also increases. The size (W/L ratio) of the transistors (N-CMOS and P-CMOS, respectively) is set to be the same, so that the comparison of power dissipation between different types of adder circuits is distinct. In our work, the clock frequency changes from 10 MHz to 1 GHz to investigate its influence on power dissipation of different types of adder circuits.

Table I : - Power consumption and Delay of existing and proposed adders circuit at 10MHz

Adder Circuit	Power (µW)	Delay pS)	PDP fWS)
C-CMOS	3.903	98.46	0.384
GDI Adder	2.449	31.48	0.077
Floating adder	3.903	12.44	0.048
Hybrid adder	4.103	6.706	0.027

Table II : - Power consumption and Delay of existing and proposed adders circuit at 200 MHz

Adder structure	Power(µW)	Delay(pS)	PDP (fWS)
C-CMOS	7.778	97.22	0.075
GDI Adder	4.966	30.26	0.150
Floating adder	6.959	6.994	0.048
Hybrid adder	8.763	6.724	0.058

Table III : - Power consumption and Delay of existing and proposed adders circuit at 1GHz

Adder structure	Power(µW)	Delay(pS)	PDP (fWS)
C-CMOS	37.31	79.5	2.966
GDI Adder	24.22	29.28	0.709
Floating adder	33.78	6.083	0.205
Hybrid adder	44.32	6.728	0.298

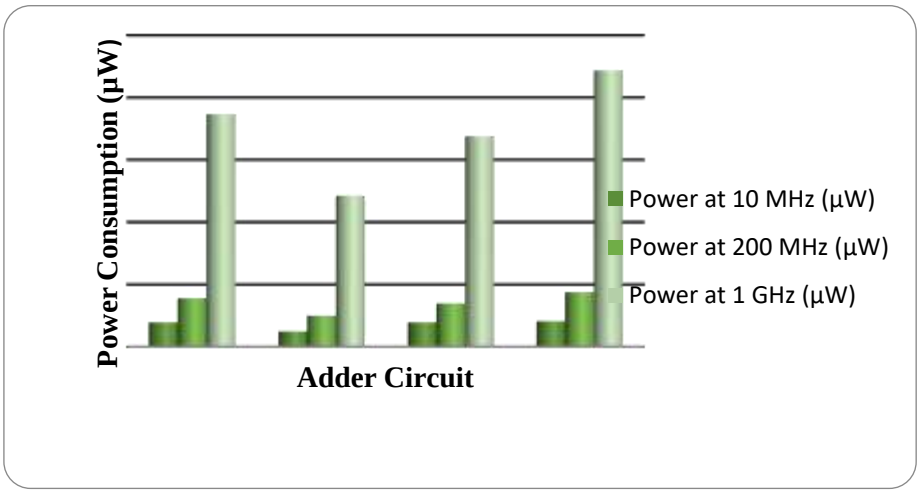

Figure.6: Comparison of power consumption by Adder circuit at different frequency

Conclusion

The primary goal of this research work has been to present a new circuit technique to improve the swing level of GDI gate along with power efficient results in digital circuit design. Design of basic cell and its fan-in and fan-

out property is also discussed. The GDI technique is suffered from low swing problem since the input voltage level at the diffusion of transistors are not fixed. Details of low threshold problem in GDI have been discussed. To overcome this problem, a swing restoring pass transistor with basic GDI technique named Hybrid GDI. The GDI technique is emerging as a strong alternative of CMOS for digital circuit design but is suffers from low threshold drop problem. Although this problem can be overcome by using buffer restoration circuits but this solution brings improvement in power and delay. The Hybrid GDI is the modification in basic GDI gates by adding single swing restoring pass transistor

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