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A LOW POWER SRAM CELL DESIGN WITH BIT-INTERLEAVING CAPABILITY IN DSM TECHNOLOGY

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Abstract
SRAM cell is the basic memory devices which is made from the combination of Flip Flop and registers for storage of data. In this paper we have proposed a novel design which exhibits lower power consumption and better stability as compared to the other existing designs when scaling of technology takes place. This proposed 11T SRAM has been compared with standard 6T SRAM, 7T SRAM cell, 8T SRAM Cell and 9T SRAM (with bit-interleaving capability) in term of Power consumption, Delay and Power Delay Product (PDP) at various supply voltages as 1.8V, 1.6V and 1.4V. For the stability analysis SNM (Static Noise Margin) also analyzed at the supply voltage 1.8V. The simulations are carried out on Cadence Virtuoso at 180nm CMOS technology and the simulation results are analyzed to verify the superiority of the proposed design over the existing designs. The higher noise margin confirms the high speed of the SRAM cell. In this paper, the proposed 11T SRAM cell shows maximum reduction in power consumption of 24.17% with 6T, of 88.6% with 7T, of 28.21% with 8T and of 35.03% with 9T, maximum reduction in delay of 9.1% with 6T, of 64.26% with 7T, of 9.18% with 8T and of 10.44% with 9T and maximum SNM of 35.02% with 6T, of 32.27% with 7T, of 34.4% with 8T and of 33.15% with 9T increases

Introduction
Low power and high speed SRAM cell has become a critical component for development of VLSI chips. This is especially true for microprocessors, where the on-chip memory cell sizes are growing with each generation to bridge the increasing divergence in the speeds of the microprocessor and the main memory. The power dissipation has become an important consideration due to the increased integration, operating speeds and the explosive growth of battery operated appliances. These on-chip memory cells are usually implemented using arrays of densely packed SRAM cells for high performance [1]. A six transistor SRAM cell (6T SRAM cell) is conventionally used as the memory cell [2]. However, the 6T SRAM cell produces a cell size an order of magnitude larger than that of a DRAM cell, which results in a low memory density [3]. Therefore, conventional SRAMs that use the 6T SRAM cell have difficulty in meeting the growing demand for a larger memory capacity in mobile applications [4]. Previous work and literature survey shows that the power dissipated by the cell is usually a significant part of the total chip power [5]. Cell accesses consume a significant fraction (30-60%) of total power dissipation in modem microprocessor [5]. A large portion of cell energy is dissipated in driving the bit-lines, which are heavily loaded with multiple storage cells [13]. Clearly, the memory cells are the most attractive targets for power reduction [11]. Besides, in cell accesses an overwhelming majority of the write and read bits are '0'. Whereas in the conventional SRAM cell because one of two bit-lines must be discharged to low regardless of written value, the power consumption in both writing '0' and '1' are the generally same [6]. In conventional SRAM cell differential read bit-line used during read operation and consequently, one of the two bit-lines must be discharged regardless of the stored data value [7]. Therefore always there are transitions on bit lines in both writing '0' and reading '0' and since in cell accesses an overwhelming the majority of the write and read bits are "0" these cause high dynamic power consumption during read/write operation in conventional SRAM cell. Furthermore, the SNMs are linearly dependent on the supply voltage, as the supply voltage is scaled down to save power the cell stability severely get affected. Hence obtaining ultra-low power consumption while maintaining the cell stability becomes the main motive of SRAM designs in this scenario. Voltage reduction along with device scaling is associated with decreasing signal charge. In this paper, a 11T SRAM cell has proposed with bit-interleaving capability with better performance. Some other SRAM cell with

bit interleaving have been presented in [6-8] in past. The proposed design has less power consumption, high speed, improved write ability, read robustness.

The brief overview of this paper as follows, in section 2 we have discussed literature review i.e. standard 6T SRAM and existing 9T SRAM cell for bit-interleaving capability has been discussed. Section 3 consists of elaboration of the proposed work, section 4 contains the simulation and results discussion and section 5 consists of conclusion part.

Literature review

SRAM or Static random Access memory is a semiconductor memory widely used in electronics, microprocessor and general computing applications. This form of semiconductor memory gains its name from the fact that data is in a static fashion, and does not need to be dynamically updated as in case of DRAM memory. While the data in the SRAM memory does not need to be refreshed dynamically, it is still volatile, meaning that when the power is removed from the memory device, the data is not held, and will disappear.

Conventional 6T SRAM Cell

The Conventional 6T SRAM cell has combination of six transistors in which four transistors (N1 P1, N2 P2) formed two inverters. These two inverters are back to back connected in cross coupled manner, apart from this two access NMOS transistors N3 and N4 acting as pass transistors and two data storing nodes (Q and QB). These data storing nodes are accessed by the pass transistor N3 and N4 as shown in Fig.1. These cross-coupled inverters forming the latch, i.e. each bit is stored in the latch. The access transistors are enabled using Word Line (WL). When the Word Line (WL) is low, access transistors are disabled and cell works in hold state, at this time read or write operations cannot be performed, at this state latch can hold bit as long as the voltages remain at V_{dd} and GND. When the word line becomes high, access transistors N3 and N4 are enabled, and at this stage read and write operations can be performed [5]. Data is write at node Q through bit line and opposite data is stored at the node QB.

They are compared with respect to power, delay and speed. Normally, the cell design must strike a balance between delay, speed, durability, cell area and leakage but power reduction is one of the most important design objectives. However, without compromising the other parameters power cannot be reduced. For the example, low-power can compromise the cell area and also the speed of operations. In Fig.1 a typical six-transistor (6T) CMOS SRAM cell is shown. Figure shows four transistors (P1, P2, N1and N2) comprise cross-coupled CMOS inverters and two NMOS transistors M5 and M6 provide read and write access to the cell. 6T CMOS SRAM cell is very famous due to its superior durability, low-voltage and low power operation.

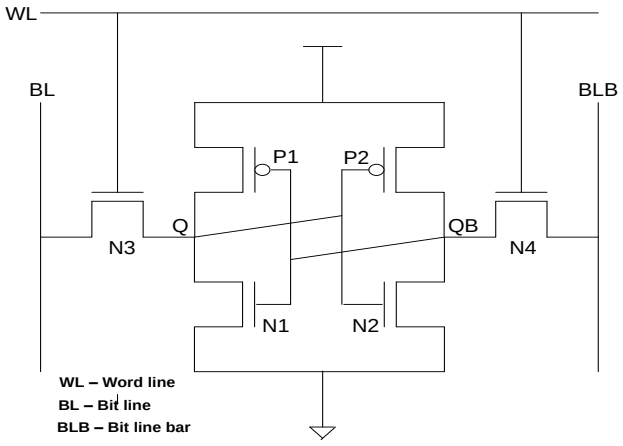


Fig.1. Conventional 6T SRAM cell

Existing 9T SRAM cell

In 9T SRAM cell three extra transistors N5, N6, P3 are added. Transistor N5 is connected between node Q and N1 for the data protection during read operation [11] , this transistor prevent the discharging of node Q since it

turn off during read , write operation . Transistor (N6, P3) forms a special inverter for AND logic operation [10] to activate local word line (LWL). It also have bit line (BL) ,world line (WL) and provide extra word line (RWL) for read operation , bit line CBLB to control transistor N5 as shown in Fig. 2 .

This 9T SRAM cell is designed with bit interleaving capability for soft error protection and this design also sort-out the problem of write 1 failure which was occurring in 6T SRAM cell. Also exhibit considerable improvement in write ability, read robustness, lower write and leakage power consumption, as well as has better tolerance in process variation [12]. Still average power and speed of the circuit can be further improved by connecting some extra transistor which is done in the proposed 11T circuit.

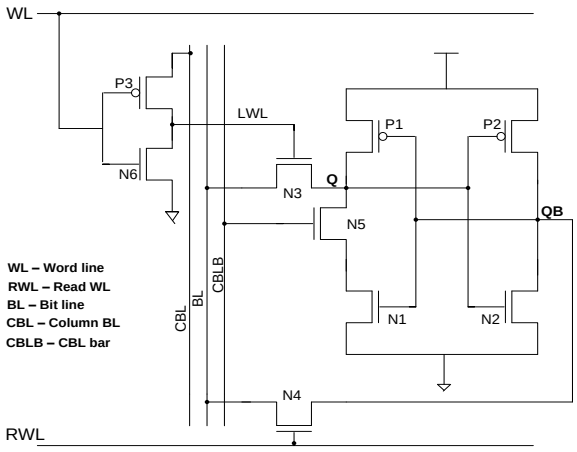


Fig. 2. 9T SARM cell

Proposed Design

Proposed 11T SRAM cell

Single ended 11T SRAM cell for bit interleaving application has been proposed, the bit interleaving idea originate from the differential 8T SRAM cell [10]. Subsequently this idea is used in read disturb free 9T SRAM cell [12]. The working of the proposed cell is a little bit similar to the 9T SRAM cell less power consumption, high speed, less PDP. The proposed SRAM cell consist of eleven transistors seven NMOS from N1 - N7 and four PMOS from P1-P4 shown in Fig. 3.

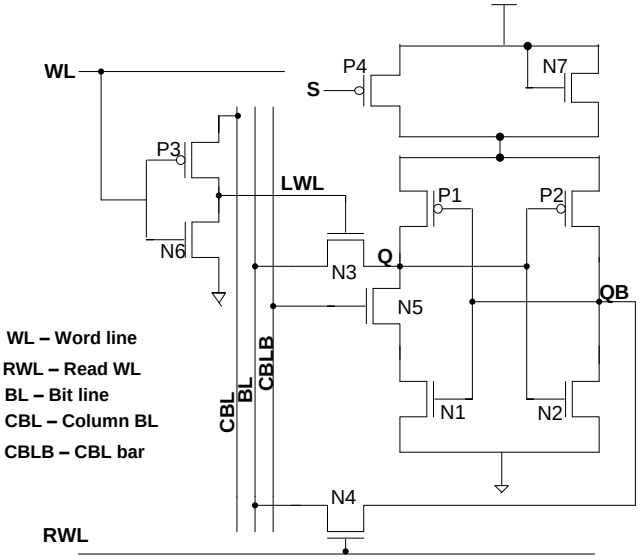


Fig.3. Proposed 11T SRAM cell

In the proposed circuit two extra transistors P4 and N7 are connected to improve the cell performances. The transistor N7 is for reducing supply voltage and transistor P4 is work as switching transistor.
The operation principle of the proposed 11T SRAM cell is discussed below.

Hold mode
In hold mode, set the word line (WL) at high voltage while RWL signal switch low, hence transistor N3 & N4 turn off to prevent the access of bit line, CBLB is set high to turn on transistor N5 as a result data retention is afforded by the cross coupled back-to- back pair .

Write Mode
In write operation pull down WL at low and enable CBL signal, then LWL signal is pre-charged to high value as a result the data is written from bit-line (BL) to storage nodes (Q & QB) through N3 .

Read mode
During read mode first of all BL is set to high , then the special read word line (RWL) signal start read operation , CBL turns high and the CBLB is turn to low voltage and WL remains at high .

From simulation result we will observed that proposed 11T SRAM cell generates Q and QB output which has proper logic without delegation of output waveform. The output waveform for proposed 11T SRAM cell is shown in Fig. 4.

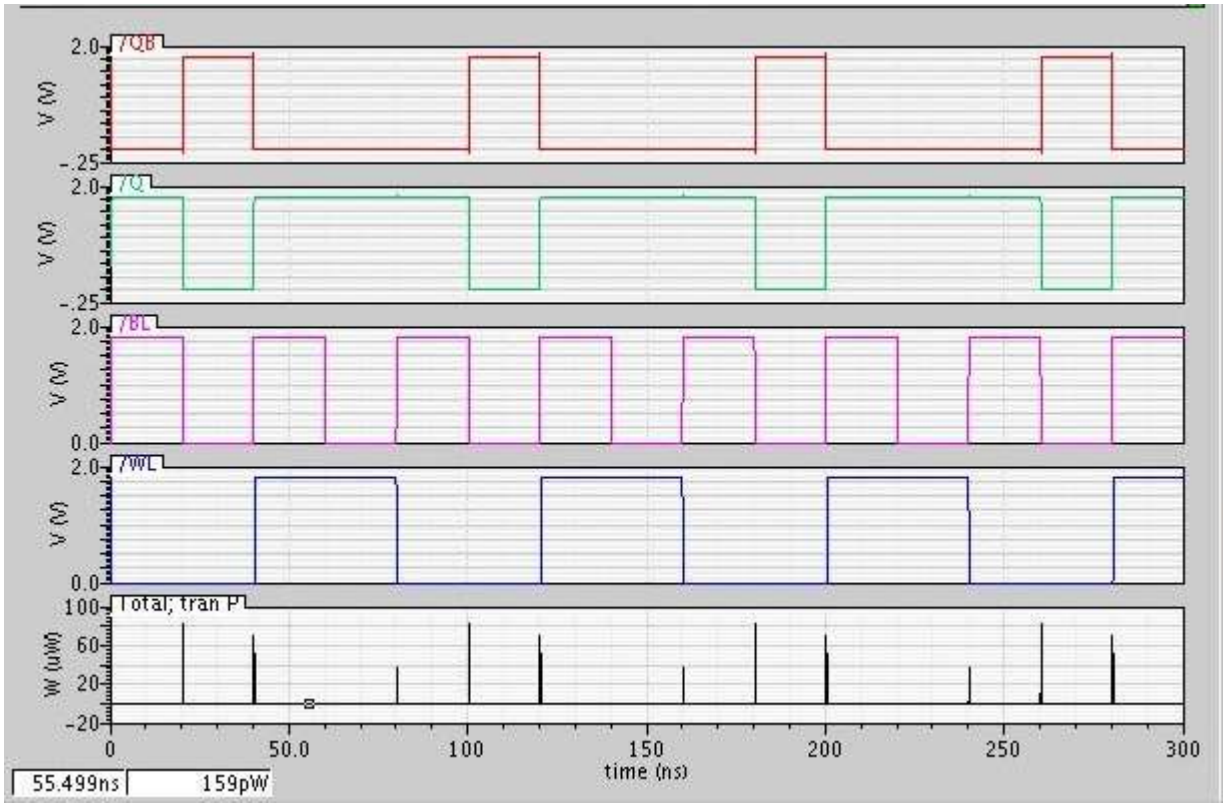


Fig.4. Output Waveform of Proposed Circuit

Bit-interleaving and shared word line architectures

Mainly two ways are used to arrange the words in SRAM architecture. Shared word line shown in Fig. 5(a) and bit interleaving shown in Fig. 5(b). A simple SRAM memory architecture as shown in Fig. 5 consists of a matrix of cells made of rows and columns. The rows are selected by the address signal generated by the row decoder. The columns are selected by the address generated by the column decoder. As shown in Fig.6 A3, A4, A5 and A6 are the address signals to select the rows and A0, A1 and A2 are the address signals to select the columns. If M X N is the size of the memory then the number of address lines needed to decode rows is 'm' where M is equal to 2m and the number address lines needed to decode columns is 'n' where N is equal to 2n [10].

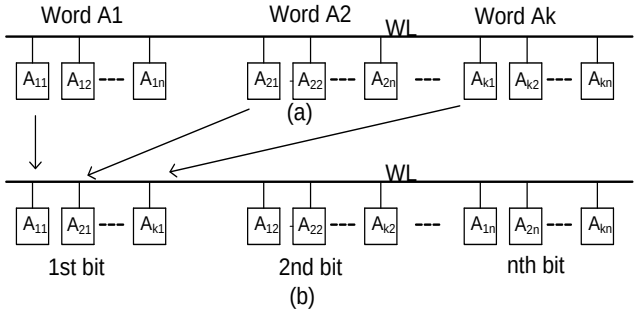


Fig.5. SRAM word organization (a) Shared word line (b) Bit-interleaving

Bit-interleaving is commonly used in SRAM design, to provide soft error protection as well as area efficient utilization of wiring. Fig. 6 shows 2x2 bit-interleaving architecture of proposed 11T SRAM cell. The detail explanations and the working of 2x2 bit-interleaving architecture is given in [12].

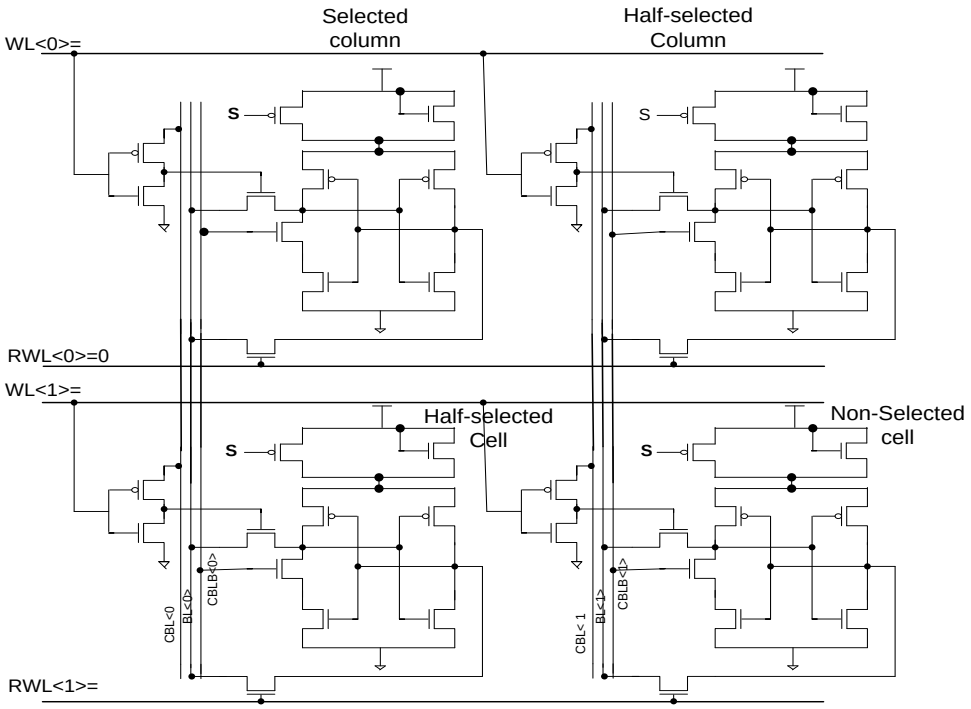


Fig.6. The 2x2 bit-interleaving architecture of 11T SRAM cell.

Cell performance analysis

In this section, cell properties such as SNM, Power consumption, delay, PDP and EDP of existing and proposed circuit at 10MHz, 200MHz and 500MHz frequency. are compared with the existing design, namely the standard 6T cell and 9T cell. All the existing and proposed circuit is simulated in Cadence Virtuoso at 180nm technology at frequency 25 MHz Power consumption and delay is calculated respectively. We observed that as we scale down the supply voltage the power consumption of the SRAM cell also reduces. The size (W/L ratio) of the transistors (N-CMOS and P-CMOS respectively) is taken to be the same for all transistor of the cell to compare different type of SRAM cell.

Speed and power analysis

The proposed SRAM cell shows 73.88% reduction in power , 71.53% reduction in PDP at 1.8V with respect to standard 6T SRAM and 9.89% reduction in power , 29.11% reduction in PDP at 1.8V with respect to existing 9T SRAM as shown in table-I. The significant improvement at other voltages can be analysed from the Table-II and Table-III. The proposed circuit has been mainly designed for bit-interleaving application with better performances compared to earlier design of 9T SRAM in term of power, speed and PDP.

Table I: - Power consumption and Delay of existing and proposed SRAM cell at 500MHz

SRAM CELL	Power(µW)	Delay(pS)	PDP (fWS)	EDE (zJ)
6T SRAM	1.504	48.12	72.37	3482
7T SRAM	1.236	56.29	69.57	3916
8T SRAM	0.952	61.39	58.44	3587
9T SRAM	0.455	63.88	29.06	1856
Proposed 11T SRAM	0.410	50.25	20.60	1035

Table II: - Power consumption and Delay of existing and proposed SRAM cell at 200MHz

SRAM CELL	Power(µW)	Delay(pS)	PDP (fWS)	EDE (zJ)
6T SRAM	1.099	55.19	60.65	3347
7T SRAM	0.893	59.29	52.94	3138
8T SRAM	0.724	65.39	47.34	3095
9T SRAM	0.337	67.89	22.87	1552
Proposed 11T SRAM	0.307	55.54	17.05	946.9

Table III: - Power consumption and Delay of existing and proposed SRAM cell at 10MHz

SRAM CELL	Power(µW)	Delay(pS)	PDP (fWS)	EDE (zJ)
6T SRAM	0.756	63.12	47.71	3011
7T SRAM	0.636	68.29	43.43	2965
8T SRAM	0.526	73.39	38.60	2832
9T SRAM	0.243	73.90	17.95	1326
Proposed 11T SRAM	0.225	62.62	14.08	881.6

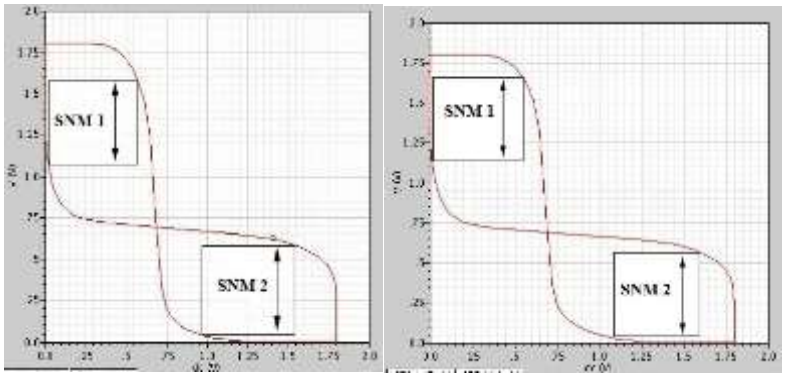
Stability Analysis

The stability of SRAM cell is defined by static noise margin (SNM); the higher the SNM the better the stability. SNM is defining maximum DC noise voltage that can be tolerate by the cell without changing the output bit or stored bit. So the cell stability is depends on supply voltage, as supply voltage is reduce the cell become less stable. The most common static approach for measuring the SNM is by using butterfly curves, which is obtain from a dc simulation. The SNM of the SRAM cell is defined as the size of the largest square that can fit into the butterfly curve [25].

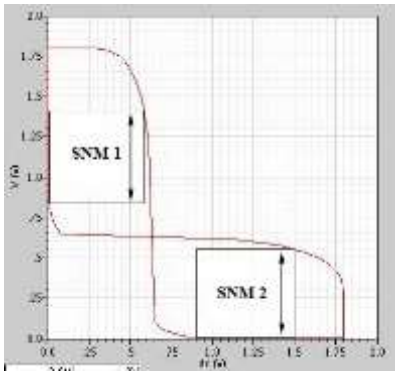
Hold stability

The hold stability of the SRAM is defined by the HSNM (Hold SNM). In 9T and proposed 11T cell the butterfly curve appear asymmetrical due to the asymmetrical stored structure. Hence the HSNM equals to the smaller one of the two maximum squares. Butterfly curves for HSNM calculation is shown in Fig. 8.

SNM = min (SNM 1, SNM 2)



(a) ***(b)***

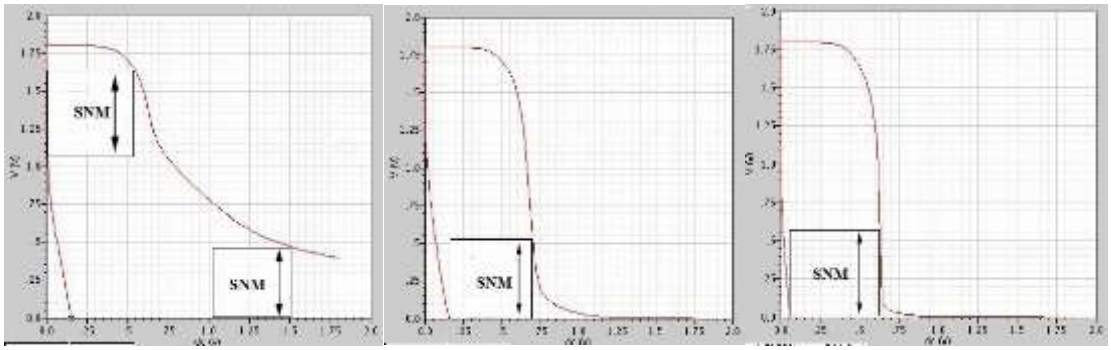


(c)

Fig.8. Statistical butterfly curves of Hold mode (a) 6T (b) 9T (c) Proposed 11T

Write stability

Write stability of SRAM cell can be analyzed by Write static Noise Margin (WSNM). The definition of the conventional WSNM based on the butterfly curve as shown in Fig.9. More WSNM shows better stability.

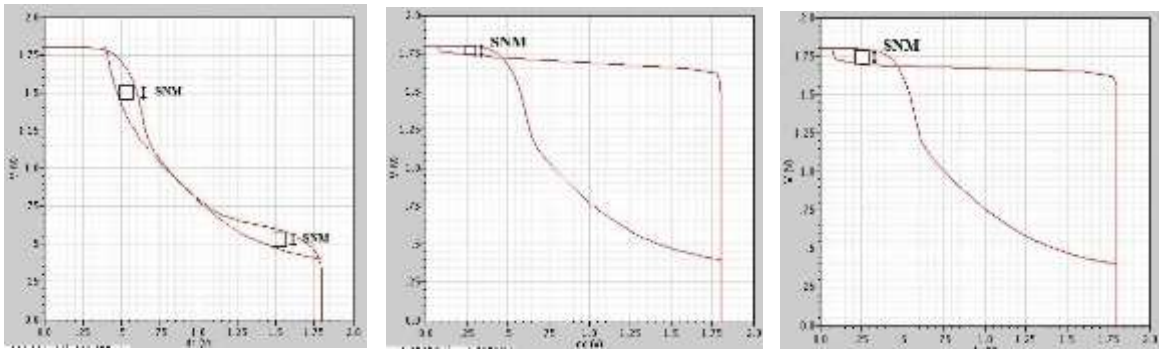


(a) *(b)* *(c)*

Fig.9. Statistical butterfly curves of write mode (a) 6T (b) 9T (c) Proposed 11T

Read stability

Read stability of SRAM cell also can be analyzed by Write static Noise Margin (WSNM). The definition of the conventional RSNM based on the butterfly curve as shown in Fig.10. More RSNM shows better the read stability.



(a) *(b)* *(c)*

Fig.10. Statistical butterfly curves of read mode (a) 6T (b) 9T (c) Proposed 11T

Comparison of the SNM of different design can be analyzed by the table IV. The table clearly shows that the proposed design has better stability as compare to 6T and 9T SRAM cell in all three modes i.e. hold mode, read mode and write mode.

Table IV: - SNM of existing and proposed SRAM cell at 1.8V

SRAM CELL	HSNM	WSNM	RSNM
6T SRAM	528 mV	460 mV	83 mV
7T SRAM	532 mV	490 mV	89 mV
8T SRAM	539 mV	521 mV	93 mV
9T SRAM	516 mV	533 mV	71 mV
Proposed 11T SRAM	558 mV	583 mV	107 mV

Conclusion

In this paper, a novel 11T SRAM cell with bit-interleaving capability has been proposed. The main motive of this paper is to reduce the power consumption, improve the stability of proposed design. Analysis of results show that, the proposed 11T SRAM cell is giving better performance in terms of stability, power consumption and PDP with respect to standard 6T SRAM cell, 7T, 8T and 9T SRAM with bit-interleaving capability. The delay of the circuit is increased slightly at the voltages above 1.8V in comparison with that of standard 6T SRAM cell but PDP of the circuit reduces in significant amount at all the voltages. While significant reduction in both delay and power consumption is observed with respect to 9T SRAM. Also the proposed circuit has bit-interleaving capability to reduce soft error probability.

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