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NEW METHODOLOGY FOR LOW POWER HIGH SPEED CLA

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Abstract

Historically, VLSI designers have focused on increasing speed and reducing the area of digital systems. Low power design reduces cooling cost is and increases reliability especially for high density systems. Moreover,it reduces the weight and size of portable devices.Yet,high performance is still the main criterion for most digital systems, which may not be sacrificed to achieve low power dissipation.This study covers two logic families; namely CMOS and CPLpresents low power digital VLSI design methodologies.To verify the qualitative analysis, three gates AND, OR, MUX are implemented using two logic families:CMOS,CPL.On the block level, a 16 bit CLA adder is used as a test vehicle to evaluate the performance of the above logic families.Then the factors like performance, Power of different CMOS logic styles is then analyzed and simulated. A 16bit CLA adder is designed,simulated, using 0.6µm CMOS technology.

Introduction

Since the invention of the first integrated circuit(IC),three decades ago,designers have been looking for methods to speed up digital circuits and to reduce the area of their designs.Recently,advances in VLSI fabrication technology have made it possible to put a complete system on a chip(SOC) which facilitates the development of Personal Digital Assistants(PDA's),cellular phones,laptops ,hand-held computers and mobile multimedia systems.The evolution of these applications profiles power dissipations a critical parameter in digital VLSI design.

Power dissipation is defined as the rate of energy delivered from the source to the system or device. Power dissipation is important for portable systems as it define the average life time of the battery.Unfortunately,battery technology is not expected to improve the battery storage capacity by more than 30% every five years.This is not sufficient to handle the increasing power requirements of portable systems.Low power devices are expected to have smaller battery size,less weight and longer battery lifetime. Another reason for low-power design arises from modern automated offices. This problem resulted in the development of the "Green Computers" concept to reduce the amount of energy consumed by office equipment.

The first half presents the various power dissipation mechanisms in CMOS digital circuits and the Effect of CMOS technology on power, delay is explained.The second half presents two famous CMOS logic styles:Conventional CMOS,Complementary Pass Logic(CPL),For each Logic styles the advantages and disadvantages are discussed with emphasis on the previous mentioned characteristics.To verify the qualitative analysis, three gates AND, OR, MUX are implemented using two logic families: CMOS,CPL. On the block level, a 16 bit CLA adder is used as a test vehicle to evaluate the performance of the above logic families.

Existing Techniques

Power dissipation is categorized in two distinct types that impact on CMOS circuits Peak power and Average Power.Peak Power: Both circuit life and performance deeply effected by Peak Power. Excessive instantaneous current drawn from the power supply results in a voltage drop over the supply rails (GND,Vdd).This large current causes a large power dissipation inside the supply wires because of their impedance. Consequently,this large power consumption causes overheating of the device which reduces the reliability and lifetime of the circuit. Also, a voltage drop along the supply lines hinders the performance of the circuit and causes erroneous digital outputs and digital glitches.Average Power:Average Power dissipation basically calculate the battery weight and lifetime. Average power categorized as dynamic power and static power.Dynamic power dissipation proportional to the operating frequency in the circuit or the frequency in node switching. Dynamic power is important during normal operation especially at high operating frequencies.Dynamic power dissipation consists of three components:Switching power, short circuit power and glitching power.The value of each of these

components is a function of the logic style used and the topology of the circuit.These components are discussed in detail in this section.

Switching power dissipation : The power consumed by the logic gate to charge the output load from the low voltage level ”0” to the high voltage output ”1” .Usually, it is independent of the logic function of the circuit.Switching power is expressed as

$$P_{switching} = F_{switching.} V_{dd}^2 . C_L$$

$F_{switching.}$ is the Switching frequency
V_{dd}^2 is the supply voltage
C_L is the net load capacitance

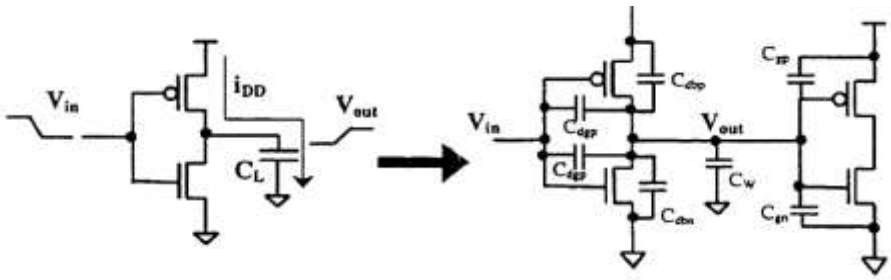


Fig 1 Sources of load capacitance in a CMOS Inverter

The net loading capacitance C_L consists of: the gate capacitance of subsequent gate(s) input(s) connected to inverter’s output, interconnect capacitance, and the diffusion capacitance of the drains of the inverter transistor. Test chips have shown that the total capacitance is split almost equally between these three types. As the minimum gate length scales down, though interconnect capacitance becomes dominant. Fig 1 shows the basic capacitive elements of a CMOS inverter.

Short circuit power dissipation : Short circuit power is the power passing from the supply to the ground during the transitions from logic “0” to logic “1” and from logic “1” to logic “0”.Unlike the switching power , which is a function of the number of “0” to “1” transitions, the short circuit power is a function of the toggling frequency. Short circuit power is either linearly or quadratically proportional to the supply voltage. And it is depends on the transistor channel length. Fig2 illustrates the output voltage of a standard CMOS inverter with the short circuit current. During transitions, both the PMOS transistor and the NMOS transistor of the inverter are ON creating a short circuit path between V_{dd} and G_{ND}.Short circuit power dissipation may be reduced to about 5 to 10% of the total power consumption of the logic circuit by proper sizing of the CMOS transistors to obtain equal rise and fall times.

P_{sc}= $I_{sc}.V_{dd}$
Isc = average short circuit current.

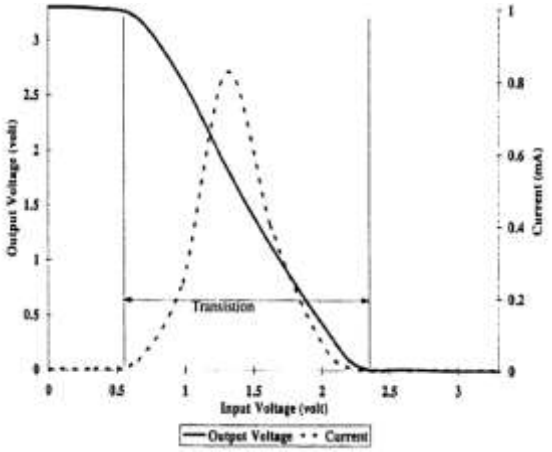


Fig 2 Output of an Inverter

Glitching Power : Glitching power is the power dissipated in intermediate transitions during the evaluation of the logic function of the circuit.

$$P_{Glitch} = V_{dd}^2 C_L . F_{Glitch}$$

F_{Glitch} – Average frequency of glitches

Power dissipation vs Delay: At the design stage Power dissipation may be reduced by using the following techniques. Parallelism, Pipelining: Power dissipation does not scale linearly withdelay .As shown in fig 3. the power dissipation verses the delay for a 32 bit CLA Adder. While optimizing the circuit for speed reduces the delay by 27%,it also increases power dissipation by 280%.If two separate adders were implemented with a delay of 1.5ns each,a better throughput with a delay of 1.5ns each, a better throughput with less power dissipation may be obtained .This is called parallelism. Pipelining partitions the logic function into cascaded series of events. The effective throughput of the pipelining is equal to the clock frequency. However the pipeline has a latency(time lapsed from first input to the first output) equal to the number of stages in the pipeline. Modern processors and microcontrollers utilize pipelining especially in instruction fetching and decoding.

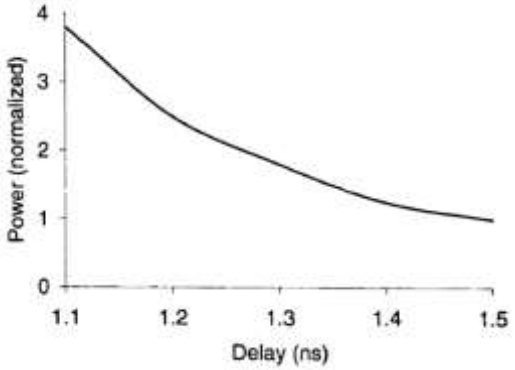


Fig 3 Power vs Delay

There are several logic families to design with but here only two logic families are explained :CMOS and CPL. Generally most logic style perform delay-power tradeoffs, but not always in proportional amounts. The best logic style is that which minimizes a constant throughput(delay).

A CPL Conventional CMOS: Conventional CMOS have been known as the logic style of choice over the last fifteen years. It is widely used in industry because of its simplicity and stability. Logic gates in conventional CMOS are constructed from an N and a P block.An AND-OR-Invert (AOI) CMOS gate is shown in Fig 4.The N block implements a sum of products function to evaluate the "0" state. The P block evaluates the "1" state of the output by implementing a product of sums function to create a path from V_{dd} to the output node. This is

equivalent to stating that the output node is always a low impedance node in steady state. Usually, each CMOS gate has 2N transistors where N is the number of gate inputs. The N and P networks are designed so that whatever the value of the inputs, one and only one of the networks is conducting steady state.The important advantage of CMOS is its robustness against voltage and transistor sizes.The percentage increase in power due to noise is low compared to other logic styles.

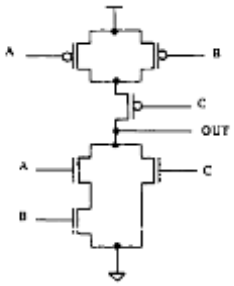


Fig 4 AOI Implemented in conventional CMOS

Complementary Pass Logic: A CPL gate consists of two NMOS logic networks(one for each signal rail),two small pull up PMOS transistors for swing restoration , and two output inverters for the complementary output signals. Fig 5 shows an AOI circuit implemented using CPL. Unlike CMOS logic, the CPL gate creates a path from the output node to one of the input nodes of the gate instead, of the power grids.

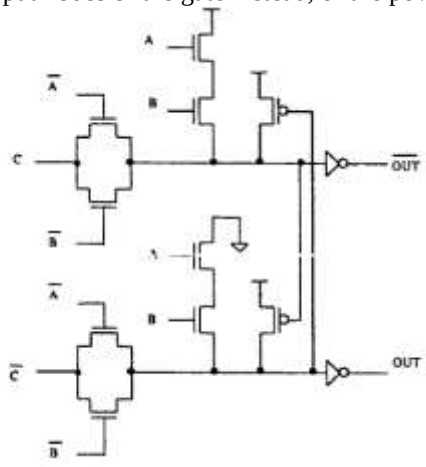


Fig 5 AOI implemented in CPL

Because the MOS networks are connected to variable gate inputs rather than constant power lines, only one signal path through each network must be active at a time, in order to avoid shorting different inputs together. Therefore, each pass transistor network realizes a multiplexer (MUX) structure.Fig6 presents a MUX implemented using CPL.The layout of pass transistor cells isnot as straightforward and efficient as CMOS, due to the irregular transistor arrangements and high density wiring.In CMOS, the layout of CMOS gates is straightforward and efficient due to complementary transistor pairs.

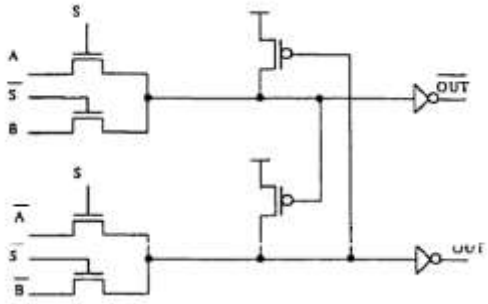


Fig6 MUX Implemented in CPL

All two input functions AND,OR,and XOR can therefore, be implemented by this basic gate structure.The overhead of this structure is relatively high for simple monotonic gates such as AND and OR.Therefore,CPL isnot recommended for simple monotonic gates.However,CPL uses smaller and fewer transistors to implement XOR and MUX based functions.Usually,CPL gates have small inputs load and good output driving capability due to the output inverters, and the fast differential stage due to the cross coupled PMOS pull up transistors.
Most CPL gates require all the inputs and their complements, which increases the routing complexity overhead. Furthermore, the wiring capacitance increases, which causes the power and delay to increase. The output voltage swing of CPL gate is lower than the input swing by the NMOS threshold voltageV_{thN},because CPL gate is constructed from NMOS only.

CLA Adder Set up

On the block level, a 16 bit CLA adder was used as a test figure for each of the two logic styles.Fig 7 illustrates the architecture of the 16 bit CLA Adder was particularly selected to compare the different logic families because of the following reasons

1. CLA adder utilizes a variety of logic gates with small and large fan-in and fan-out gates.It also includes simple gates (AND and XOR)
2. CLA Adder is not a regular architecture. Therefore ,it is good example for an arbitrary logic circuit.

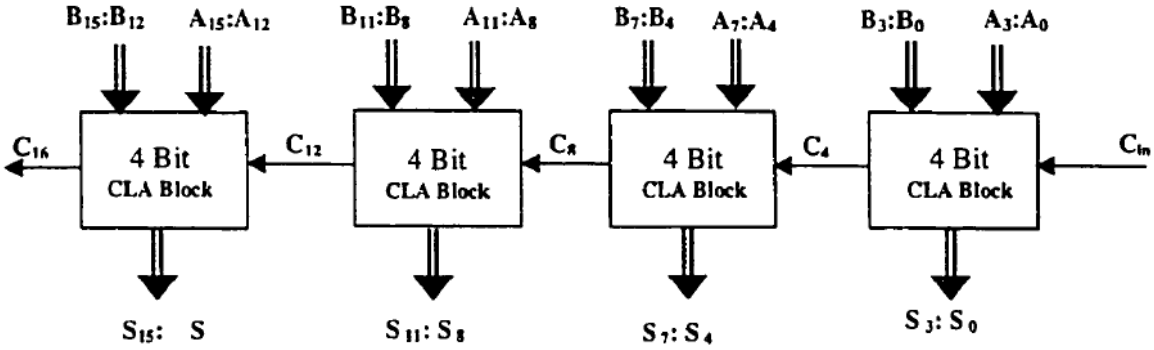


Fig7 Architecture of a 16 bit CLA Adder

The critical path delay of the CLA was calculated , where the carry propagated through the four "4bit CLA adder"

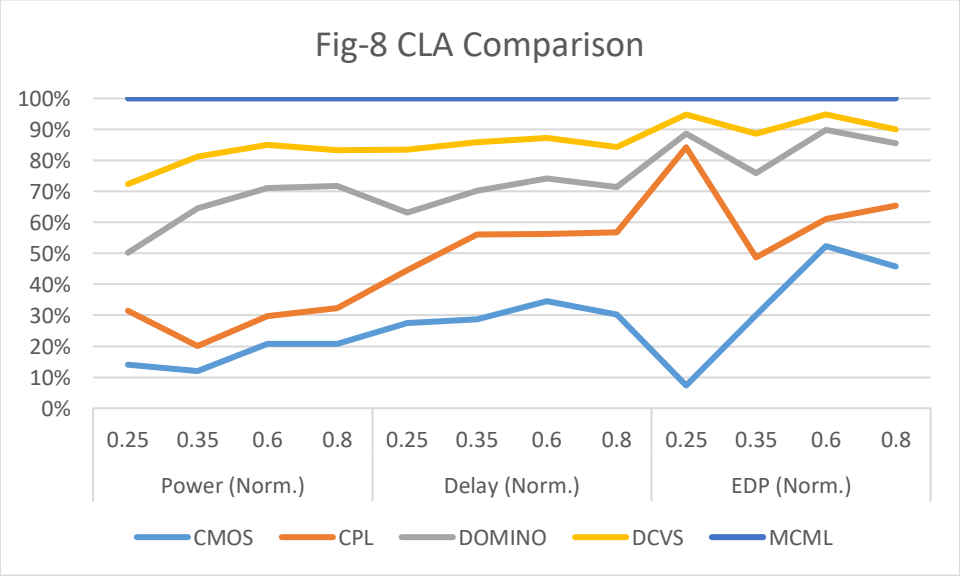
Table-1 CLA Comparison

Logic Style	Power (Norm.)				Delay (Norm.)				EDP (Norm.)			
	0.25	0.35	0.6	0.8	0.25	0.35	0.6	0.8	0.25	0.35	0.6	0.8
CMOS	1	2.12	5.82	26.6	1	1.65	3.1	3.62	1	5.78	56	348
CPL	1.23	1.43	2.49	14.8	0.62	1.58	1.95	3.16	10.48	3.57	9.4	148
DOMINO	1.33	7.86	11.6	50.5	0.67	0.81	1.62	1.75	0.59	5.2	30.7	154
DCVS	1.57	2.96	3.9	14.6	0.74	0.91	1.17	1.54	0.85	2.46	5.3	34.2
MCML	1.96	3.31	4.22	21.5	0.6	0.81	1.15	1.88	0.71	2.17	5.58	75.4

Results and Analysis

Table 1 shows results of the CLA adder. The normalized power, delay and EDP are indicated. It is clear from the table that Conventional CMOS implementations have the worst delay for all technology generations, and attains average power dissipation. CMOS delay is high because the critical path in the CLA adder has complex gates which are not suitable for CMOS. The power dissipation is high because of the high glitching activity, due to the large logic depth of the adder. Conventional CMOS is therefore, the least efficient way to implement the CLA adder. Domino to logic comes as the second worst implementation because of using NP-to implement the XOR gates.

The differential logic structures have better EDP value. This occurs because of the many AOI and XOR structures that are used to build the CLA adder. It should be noted that in the implementation of the CLA using CPL logic, each gate was built using only one logic branch to reduce the power dissipation.



Conclusion

Many factors are important in optimizing MOS transistor performance. Gate oxide thickness should be as thin as possible to improve short channel characteristics, maximize the drain current, and facilitate supply voltage scaling for reduced power. However, the minimum gate oxide thickness is dedicated by reliability, defect density, and the gate capacitance considerations. Threshold voltage should also be set low to maximize the drain

current and to facilitate the reduced supply voltage, but not low as to increase the OFF current and standby power to unacceptable levels or to result in functional failure of dynamic circuits.

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