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DESIGN OF CURRENT MODE MULTIPLIER/DIVIDER CIRCUIT USING A CURRENT DIFFERENCING BUFFERED AMPLIFIER

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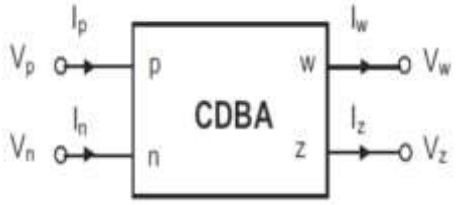
Abstract
A design of multiplier/divider circuit using a single Current Differencing Buffered Amplifier (CDBA) is presented. Here the objective is to simultaneously realize a multiplier and a divider without changing the circuit configuration which achieves less power consumption. It uses the Trans Linear technique to find out the theoretical output of the circuit. Here the current mode approach is used which is suitable for low voltage high speed analog circuit design. The proposed structure is implemented in 180-nm CMOS technology in cadence virtuoso environment. The power consumption is found to be reduced whose value is 45.67µw and the bandwidth of the designed circuit is found to be improved whose value is 83.6 MHz.It achieves more simplicity and flexibility compared to existing designs and is free from parasitic capacitance.

Introduction
Multiplier and divider circuits are widely used in analog signal processing structures in the area of analog integrated circuit analysis and design. The simple architectures of multiplier/dividers [1]–[4] are designed based on subthreshold operated MOS transistors. By using the squaring characteristic of MOS transistors biased in saturation, multiplier is designed to improve -3db bandwidth [5]. Improved accuracy multiplier circuit [6] is designed based on functional basis for implementing function synthesizer circuit. Many researchers have designed analog multiplier/divider circuit using a variety of active elements such as Current Controlled Current Conveyors (CCCII), second generation Current Conveyors (CCII), Operational Trans conductance Amplifier (OTA) [7].Multiplier and divider circuits are designed using Floating Gate MOSFET (FGMOS) require less supply voltage and power requirement [14]. Other method in designing multiplier circuit uses translinear loop concept and squaring characteristics [15].

In this paper multiplier circuit is designed using Current Differencing Buffered Amplifier (CDBA).Generally opamp based circuit have several drawbacks because of low bandwidth and slew rate. In order to overcome these drawbacks current mode approach is used for high speed systems. In recent times a new active building block called CDBA is used widely because of its simple implementation. CDBA have received significant attention because it offers lot of flexibility and versatility in analog circuit design. It also offers high slew rate, wide bandwidth and high frequency. Inthis paper a new CDBA-based circuit is proposed which consists of a single CDBA along with only six MOSFETs and offers the significant advantages like simultaneously realizing multiplier as well as a divider from the same configuration and the output of the configuration is independent from the aspect ratios of the MOSFETs if all of them are assumed to be matched. There are different ways to design a CDBA. One of the possible realizations is by using a Current Feedback Operational Amplifier (CFOA). There are also other implementations which are suitable for bipolar technology.

Current differencing buffered amplifier



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The circuit symbol of CDBA is shown in Fig. 1, where p and n are input terminals, w and z are output terminals.It is a multi terminal component with two inputs and two outputs.

Ideal voltage and current characteristics of the CDBA is given by

$$V_P = 0,\ V_n = 0,\ I_Z = I_P - I_n,\ V_W = V_Z \qquad (1)$$

By taking the non idealities into account, equation (1) becomes

$$V_P = 0,\ V_n = 0,\ I_Z = \alpha_P I_P - \alpha_n I_n,\ V_W = \beta V_Z \qquad (2)$$

Where α_P and α_n are the current gains and β is the voltage gain.The current through z-terminal is the difference of current through p- and n- input terminals. Here p- and n- are inverting and non- inverting input terminals respectively. The z-terminal is called the current output and w-terminal is called the voltage output since it follows the voltage output of z. Since the difference of input currents are converted into a voltage V_w, CDBA can be considered as a special type of current feedback amplifier with differential current input and grounded y input. The input currents i_p and i_n are internally grounded thus the input impedance of the terminals p and n are ideally zero. It is implemented using MOS as shown in Fig2

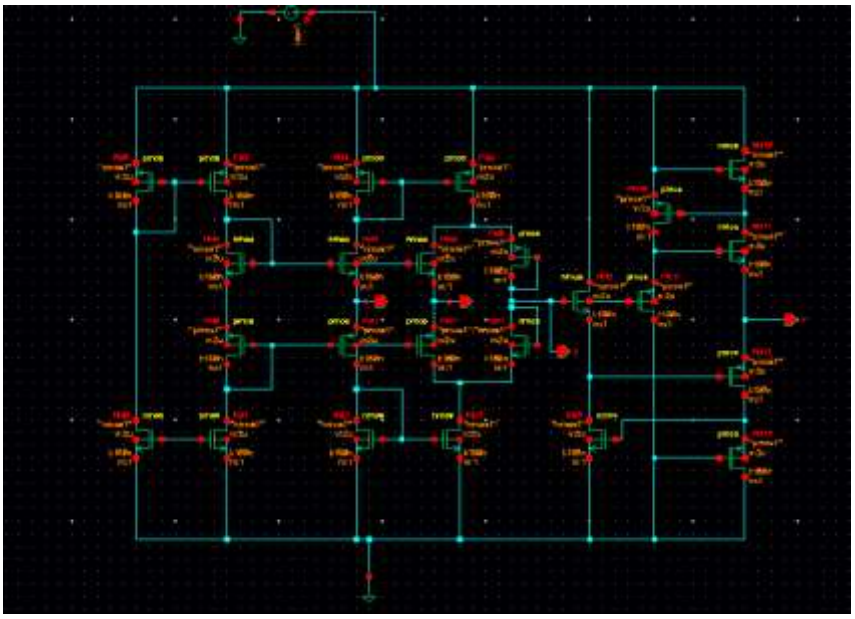

Fig 2. Implementation of CDBA using MOS

It consists of a Differential Current Controlled Current Source (DCCCS) which has a finite input resistance followed by a voltage buffer. It can be operate in both voltage and current mode. In Fig 2, M1-M16 forms DCCCS circuit and MB1-MB8 forms voltage buffer circuit.

In the ideal case the transfer function of the circuit can be expressed by

$$T(S) = \frac{Iout}{Iin} = \frac{Yp - Yn}{Yp + Yn} \qquad (3)$$

This form of $T(S)$ is suitable for first order all pass filter applications. Here the singleCDBA along with six MOS transistors is used and provides a single ended voltage output. To obtain a differential output voltage the other multiplier circuits uses two squaring circuits along withresistors. Here the same task is performed with only six MOSFETs and a CDBA element. Many applications are based on CDBA namely fully integrated signal process circuits, current mode filters, voltage mode filters, resistance controlled sinusoidal oscillators.

Theoretical analysis

Proposed implementation of current-mode multiplier and divider circuit is presented in Fig. 3, 4. Translinear loop is a loop that goes through only source-gate connection of MOS. Here the translinear loop exists in M1, M2, M3,and M4 transistors and their gate -source voltages can be expressed as follows:

$$2V_{GS}(I_2) = V_{GS}(I_{D1,2}) + V_{GS}[I_{D1,2} + 2(I_1 \pm I_0)] \qquad (4)$$

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The drain current is assumed to be proportional to the square of the weighted sum of the input signals which considers the squaring characteristics of MOS biased in saturation. The drain current is expressed as,

$$I_{D1,2} = I2 - (I_1 \pm I_0) + [(I_1 \pm I_0)_2 / 4I_2] \quad (5)$$

Thus the output current expression is

$$I_{OUT} = I_{D2} - I_{D1} + 2I_0 \quad (6)$$

Which results,

$$I_{OUT} = I_0 I_1 / I_2 \quad (7)$$

Hence both multiplying and dividing function can be implemented, which has the advantage of independency of output current on technological parameter and it is not affected by temperature variations. For a MOS transistors mobility degradation can be modeled as

$$\mu = \frac{\mu_0}{(1+\theta(v_{gs}-v_t)} \quad (8)$$

Here θ is a mobility reduction parameter which is process dependent and may have values ranging from 0.01 to 0.25 V^{-1}. Mobility reduction is considered to be geometry independent and causes more problems for distortion.

Implementations and results

A complete multiplier and divider circuit using CDBA element is shown in Fig 3. It can be able to operate as a multiplier and the divider without changing circuit configuration. There are three input terminals in the circuit namely X, Y, Z. To operate the circuit as a multiplier, input signals are applied to X and Y terminals and the control voltage is applied to Z terminal. The input signals are varied from -0.2 mA to 0.2 mA. The control voltage Ic1 and Ic2 is 1.2 mA, 1 mA.Similarly to operate the circuit as a divider, input signals are applied to Y and Z terminal which varies from -0.2 mA to 0.2 mA and -2 mA to 2mA respectively. The control voltage is applied to X terminal and its value is similar to a multiplier. Hence by changing inputs to different terminals, two modes of operation can be done.The output current of the analog multiplier is given by

$$Io\ mul = \frac{xy}{(Ic2-Ic1)} \quad (9)$$

The output voltage of the analog divider is given by

$$Io\ div = (Ic2 - Ic1)\frac{y}{z} \quad (10)$$

The circuit configuration has independence of output from the aspect ratios of the MOSFETs if all of them are assumed to be matched. On the other hand different aspect ratios are used for input and output MOS transistors to have desired gain factor

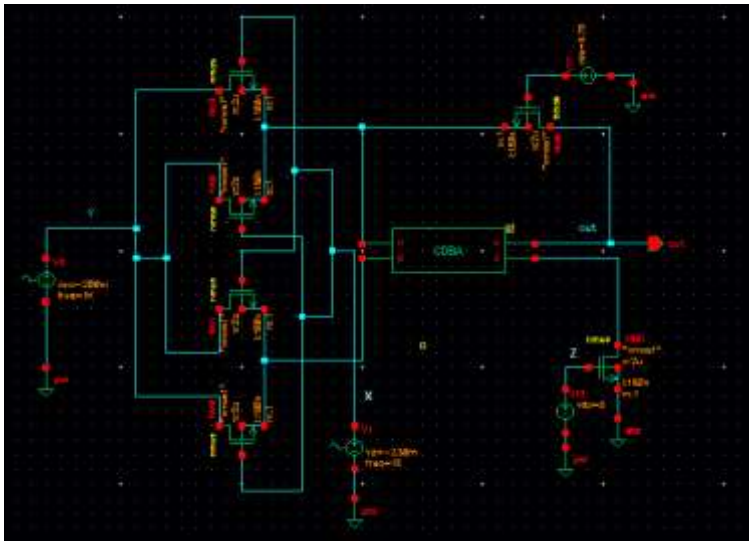

Fig 3. Implementation of Multiplier Circuit

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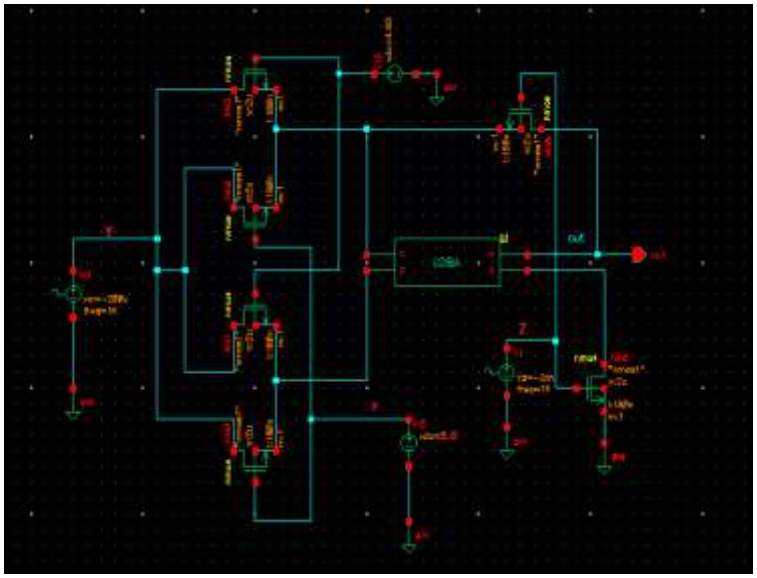

Fig 4. Implementation of Divider circuit

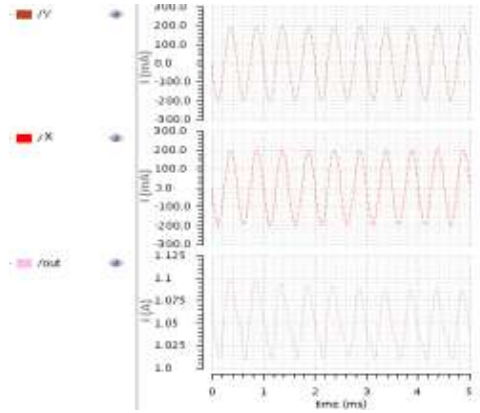

Fig 5a. Transient response for the multiplier circuit

From the Fig 5a, the output of the multiplier circuit is calculated for the corresponding inputs with respect to time

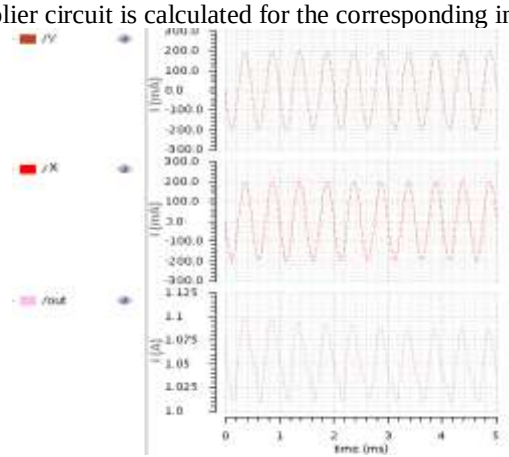

Fig 5b. AC response for the multiplier circuit

From the Fig 5b, the magnitude of the multiplier circuit is calculated with respect to the frequency.

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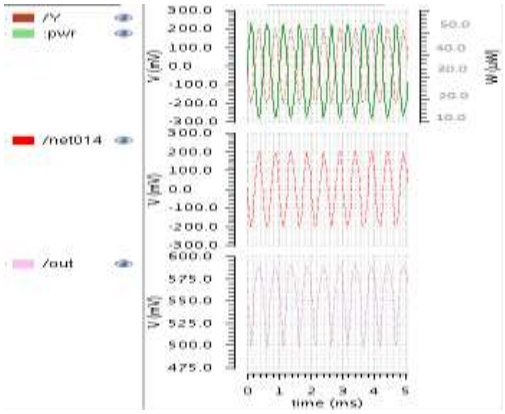

Fig 6a. Power response of the circuit

From the Fig 6a, the average power consumption of the circuit is calculated.

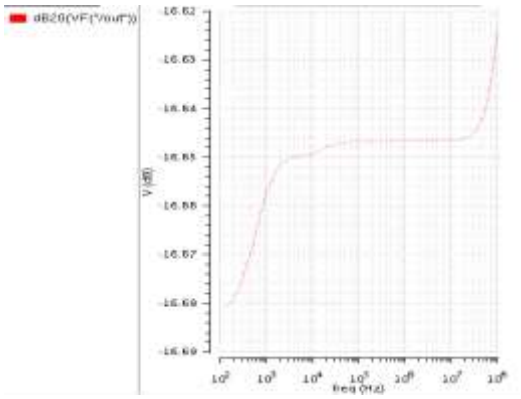

Fig 6b.dB waveform

From the Fig 6b, the bandwidth of the circuit is calculated.

Table1

Comparison between the proposed multiplier/divider circuits and previous reported works

Reference. No	Technology (µm)	Supply voltage (V)	Power consumption (µW)	Chip area (µm^2)	Bandwidth (MHz)
[5]	0.8	1.75			0.2
[6]	0.35	2	5.5	18700	4.3
[8]	0.35	1.2	130		
[10]	0.35	1.15	290		44.9
[14]	0.18	1.2	60	600	79.6
Fig 3	0.18	1.2	45.67		83.6

From the table of comparison, we can compare the parameters like technology, supply voltage, power consumption, and the bandwidth between the existing and the proposed techniques

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Conclusion

This brief presented the current-mode multiplier/divider circuit designed using Current Differencing Buffered Amplifier (CDBA). The presented structure reduces the circuit's power consumption of about 45.67µW and improves the bandwidth of about 83.6 MHz and also simplifies the implementation. It can be able to operation the frequency range of more than 100 MHz. The proposed structure uses only six MOSFET's along with CDBA. Implemented circuit using 180-nm CMOS technology has the advantage of realizing both multiplier and the divider in the same circuit.

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