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SENSE AMPLIFIED DIFFERENTIAL GATED FLIP-FLOP FOR POWER SAVING & SINGLE INTERGITY

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Keywords: Clock Skew, Differential Gated, H-clock tree, Resonant clocking, SAGFF clocked flip-flop,NOR Gating.

Abstract

The clock distribution network mainly comprises of the clock tree and the flip-flops. The resonant clocking, which drives the clock tree retains a huge potential for anextensive power minimization in the clock distribution network. In addition, the clocked flip-flops, being critical timing elements in the clock distribution circuitry, have become a major contributor to the total power dissipation. Thus, firstly, this paper proposes the design of a novel flip-flop called Sense AmplifiedDifferential Gated Flip Flop (SADGFF). The resonant clock of the design controls the timing of the circuit. This type of semi adiabaticmaneuver is proved to reduce the dynamic power dissipation in the proposed design by 26%. Further, the proposed clocked flip-flop achieves a negative setup time, and this factor makes the design extra tolerant to the clock skew and the jitter. This also reduces the D-Q delay, thus refining the timing performance of the flip-flop. Hence, the new clocked energy recovery flip-flop (SADGFF) proves to be a robust, power efficient and performance competent design that eliminates the issues of the existing differential clocked flip-flops. Secondly, this paper also investigates the use of the resonant clock in a Hierarchicalclock tree distribution network operating the flip-flops at its leaf node. The advantages of SADGFF clocked flip-flop are validated through exhaustive simulations and comparisons with the SAER and SDER flip-flop structures available in the literature.
Furthermore, the post-layout simulations of a typical H-clock tree driving 1024 leaf-cells containing flip-flops have beencarried out. Cadence® EDA tools and the 45nm process technology files have been used to substantiate the merits of the proposed design.

Introduction

A major contributor to the total power in modern microprocessors is the clock distribution network, which can dissipate as much as 70% of the total power for high-performance applications [1]. Further, the increased complexity and the challenging performance in high speed VLSI systems increase the clock load, which aggravates the clock power dissipation. This aspect persuades the researchers and designers to find novel low-power solutions for the clock distribution, to enable the rise in chip functionality. As a set of promising low-power clocking solutions, energy recovering clocking techniques have emerged in the literature [1][2][3].
One of such techniques is the resonance based clocking, which is proved to bring the clock tree power down to a bare minimum. It employs the energy recovery type clock driver for driving the clock tree. This method gains increasing research interest, since the resonant clocking recycles or recovers most of the energy used in charging the clock tree nodal capacitances. Secondly, the crucial timing elements in the synchronous digital systems are the latches and the flip-flops. They constitute the clocked registers of the clocked distribution networks that synchronize the data flow of the VLSIcircuit. These clocked flip-flops consume a substantial fraction of the clock-cycle time, and they hence dissipate considerable portion of 35% of the total power [2]. Moreover, the timing characteristics of the clocked flip-flops are extremely important, since the timing influences the performance of a synchronous system directly. Ideally, all the clocked flip-flops of a synchronous design are anticipated to receive the clock signal simultaneously. However, the parasitic effects incurred in the distribution of the clock signals, and to various degrees by the interconnects across the chip, and several limitations emerging due to these factors usually result in non-idealities of the clock distribution. They may cause temporal and spatial variations in the clock signal resulting in apparent clock skew and jitter [3]. However, its required that the synchronization circuits such as the clocked flip-flops should contribute for, as little latency as possible and incur lower power dissipation. Hence, it becomes absolutely essential to focus on both the power efficiency and signal integrity of the clock synchronization circuits. Thus, this paper proposes a new Sense Amplified Differential Gated Flip Flop (SADGFF) structure with the following features

1. Capability to exhibit sturdiness to clock skew and jitter
2. Power efficient
3. Incur reduced propagation delay
4. Design that removes the problems of charge leakage, floating nodes and charge sharing.

In addition, the local clock inverter of the native design is replaced with a differential gating NOR structure that is proved to reduce the clock switching power in the idle mode. This paper also explores Hierarchical clock tree distribution structure with 16 clock nodes. With the use of resonant clocking in the H-clock tree to drive the clocked flip-flops at its1024 leaf ends. Section II presents a brief discussion of various differential clocked flip-flops found in the literature. It highlights the choice of design aspects followed, which assert their improved power and performance characteristics. Section III explains the proposed Sense

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Amplified Differential Gated Flip Flop (SADGFF) clocked flip-flop structure, the design traits, its operation and the comparative merits. The section also does not elaborate the differential gating NOR structure and the benefits derived in the novel flip-flop.

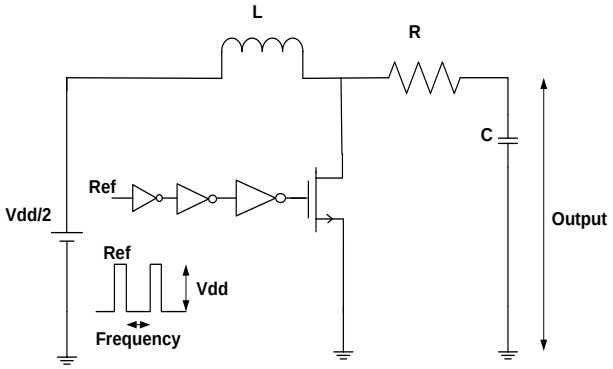

Fig. 1. Resonant Clock Generator.

The analytical justification and reasoning of the various features of the proposed flip-flop are also discussed inthe section. Section IV presents the hierarchical clock tree distribution structure used to drive the clocked flip-flops inthe 16 clock nodes. Section V presents the simulation results with the necessary graphical plots illustrating the benefits of the proposed design. Section VI concludes with the future scope of the present work.

Energy recovers clocking and clocked flip-flops

In a synchronous digital system, the clock signal is used to define the time reference for the movement of data within the entire system. The clock distribution network distributes the clock signal(s) from a common point to all the timing elements that require the clock for synchronization. In this process, it consumes a major fraction of the total power. Hence, an appropriate solution to this issue would be the use of a resonant clock. Such a power clock signal maybe sinusoidal or trapezoidal in shape, with the inherent circuit characteristics to recover all or part of the energy used in charging the clock nodes [4]. A typical circuit for the resonant clock generation is shown in Fig. 1.

Clock distribution based on such resonating drivers has been shown to be advantageous in terms of signal integrity too [5]. To derive the maximum advantage of the resonant clocking approach, the clock signal needs to be driving the clock network without any intermediate buffering. Hence, the clocked elements, like flip-flops and latches, must be clocked with the output of the clock generator directly [6]. Secondly, the adiabatic principle of charging a node capacitance has the potential to reduce the power dissipation well below the conventional $f.CV^2$relationship [5]. Flip-flops and latches optimized and adapted to a sinusoidal clock exist in the resonant clocking literature. They are Sense Amplifier Energy Recovery flip-flop (SAER),Static Differential Energy Recovery flip-flop (SDER), Single-Ended Conditional Capturing Energy Recovery flip-flop (SCCER), Differential-Ended Conditional Capturing Energy Recovery flip-flop (DCCER) as shown in Figs. 2(a)., 2(b)., 2(c).and 2(d). Respectively [7].

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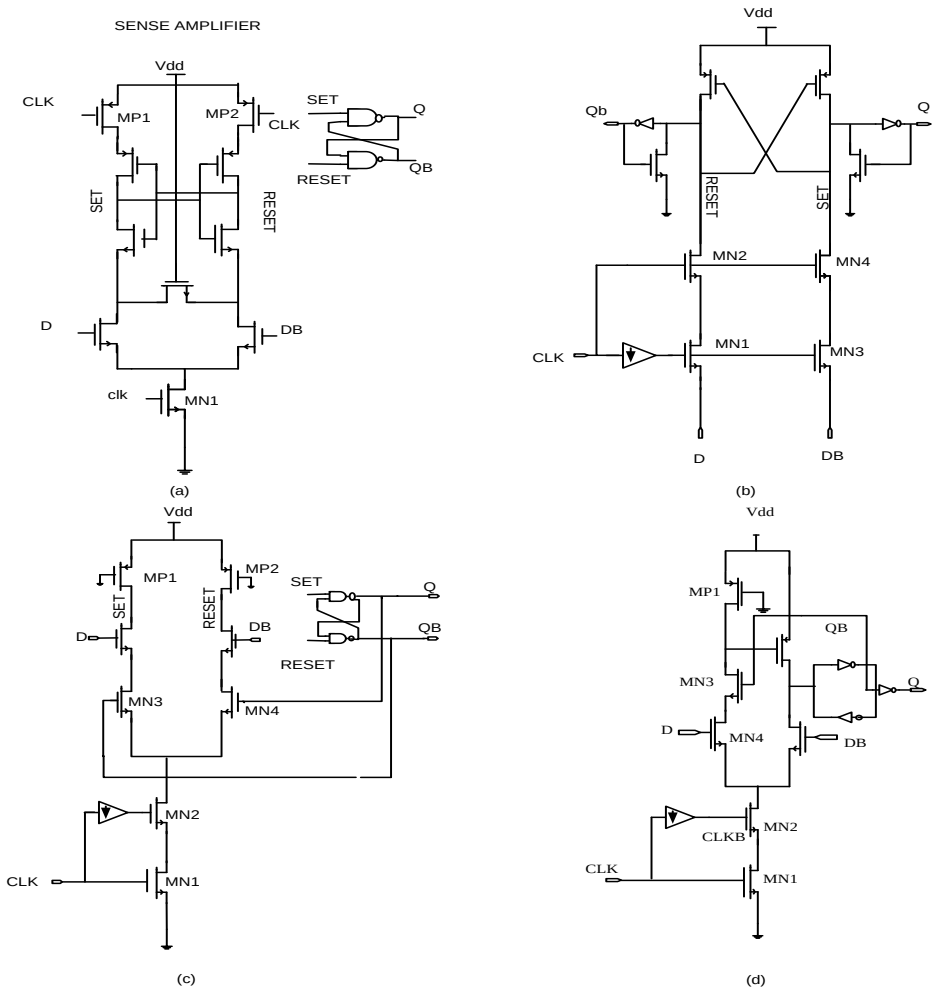

Fig. 2. Energy recovery Flip Flop.

The sense amplifier Energy Recovery Flip-Flop (SAER) [8] shown in Fig.2(a). has been acclaimed for faster operation evenwhile operating at lower power dissipation. However, its nodes *set* and *reset* are continuously in *precharge*conditioneven for low data switching activity conditions. To rectify the above drawback, either a static flip-flop may be used or the structure can adopt conditional capturing and evaluation strategies. Due to the slow transition time of energy recovery clock, high threshold prechargetransistors are found to be used in the design, without which the flip-flop may result in increased short circuit current.

Static Differential Energy Recovery Flip-Flop (SDER) [8] has a minimum sized inverter skewed for sharper high to lowtransition for the proper operation of the flip-flop. The transistors MN1, MN2, MN3 and MMN5 of Fig. 2b are made to conduct fora short time, during the rising transition of the clock and when both the CLK and CLKB are above the threshold ofNMOS. It does not require precharging, as the *set* and *reset* nodes are retaining the state statically. There is noswitching when the data is idle. Further, when the data is same as the previous, the internal switching is eliminated [8].

All this has been shown to result in considerable power dissipation reduction. The flip-flop in Fig. 2d is the Differential Conditional Capture (DCCER) flip-flop and is a dynamic flip-flop that eliminates the redundant internal transition with conditional capturing [9]. Precharging transistors *MP1* and *MP2* are used for precharging and NAND based latch is used for storage. The Q and QB output control the evaluation path of *MN3* and *MN4* for conditional capturing. Single Ended Conditional Capturing flip-flop (SCCER) is the single ended version of DCCER [10]. The *MN3* transistor providesconditional capturing. The right side is the state evaluation path with conditional capturing. Stacking *MN3* above *MN4* hasbeen aimed to reduce the charge sharing.

The proposed Sense Amplified Differential Gated Flip Flop (SADGFF) is shown in Fig.3. This flip-flop design is a quasiadiabaticstructure, employing the resonant clocking. It is proved to be more power efficient, with reduced delay in comparison to the existing differential clocked flip-flops. It also mitigates the commonly found adverse effects, namely, the charge leakage, charge sharing, floating nodes, clock skew and clock jitter issues found in conventional flip-flops asI will be discussed in detail in the following section.

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Proposed SADGFF clocked flip-flop structure

AfterThe sense amplified differential gated flip-flop consists of the pull up network of cross-coupled *PMOS* transistors *MP1*and *MP2*. The pull down network is composed of *NMOS* transistors *MN1*, *MN2*, *MN3*and *MN4*. The clocked transistor *MN4* is fed with the resonant clock *PCLK* at its gate terminal. The device *MN3*is supplied with the inverted and gated *PCLKB* signal at its gate. *ENABLE is* the Enable signal for the NOR gate. *MN5*and *MN6*are the low impedance transistors to prevent the floating nodes. Further, the charge leakage which may happen after the evaluate between the pulses due to the leakage currents is avoided due to the stacked transistors *MN1*,*MN3*and *MN4*/ *(MN2*, *MN3*and *MN4*). However, it may be argued that the stacked transistors in the evaluation path may result in charge sharing when all the three transistors are simultaneously *ON*. To keep the change in the output node voltage $\Delta VOUT$ less than the *NMOS* threshold *Vth*, properly sized NMOS transistor have been employed*MN4>MN3>MN1*/*MN4>MN3>MN2*. The following section details the NOR-gated structure.

Differential gating NOR structure

It is known that the clock signal is the single signal in any synchronous design, which has an activity ratio of 1. In other words, the clock signal switches all the time. Thus, significant power is being wasted during the transitions within the switching blocks, even when the output/input from/to the block is not needed, or when there is no input data activity. These observations led to the power saving technique in the SADGFF clocked flip-flop called as clock-gating. It involves the addition of certain logic gates to the clocked flip-flops, such that portions of the flip-flops can be turned off when not needed [10]. This is realized through selectively allowing the clock signals to the data circuits.

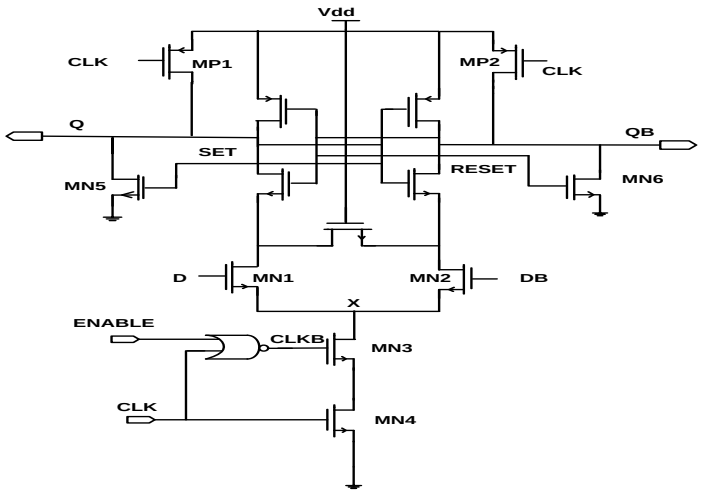

Fig. 3. Sense Amplified Differential Gated Flip Flop (SADGFF).

In the conventional timing elements, the square wave clocking is implemented through the use of clock gating byintroducing an AND logic gate or by masking the clock, at any arbitrary node of the clock network [10]. In such cases,energy recovery is not thus possible from the clock tree. Furthermore, the insertion of such a masking AND gate on thepath of the sinusoidal clock, destroys the shape of the clock itself in the clock distribution network. It also hinders theenergy recovery from the downstream fan-out capacitances of the clock network. Hence, this work implements theclock gating by inserting the gating feature inside flip-flops themselves, in a fine-grain approach.

Clock gating is made through replacing the inverter proposed in reference [9] with the NOR gate as shown inthe Fig.4(a). The NOR gate has two inputs, namely, the clock signal and the enable signal *Enable*. Fig. 4(b).depicts thesignal transients of

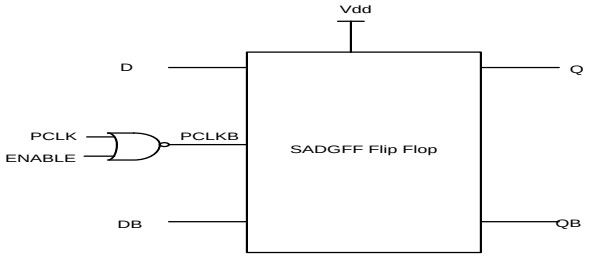

Fig. 4(a).Self-Gated NOR Gating.

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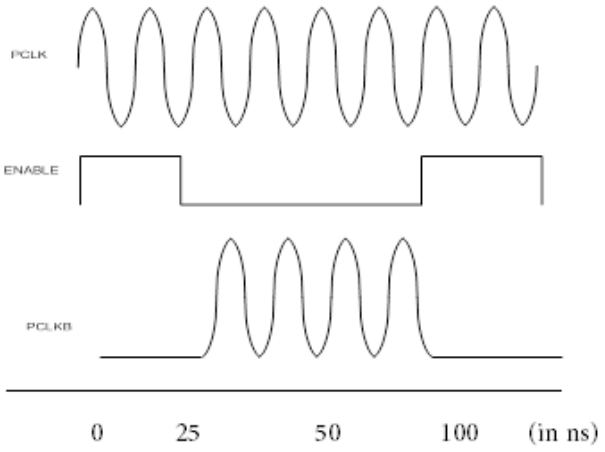

Fig. 4(b). Clock Gating Input and Output.

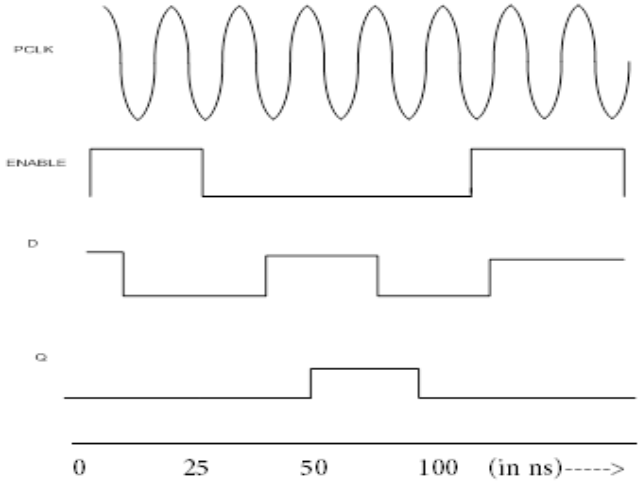

Fig. 4(c). Simulated input and output waveforms of the SADGFF flip-flop in Cadence® spectre environment.

the NOR gated structure. Here, the enable signal is made active low. When the En signal is low, thePCLK applied at its second input is applied as inverted power-clock PCLKB as shown in Fig. 4b. Similarly, when En ishigh, it gates the signal PCLK, and hence, disables the device *MN3*. In other words, in the idle state, the enable signal Enis set to *high*. This disables the internal clock by setting the output of the NOR gate to zero. This turns *off* the pull downpath of the SADGFF clocked flip-flop through transistor *MN5*. It prevents any evaluation of the data input, if applied.

Operation of the proposed SADGFF clocked flip-flop

Figure 4c shows the signal transients at the input and output nodes of the flip-flop structure. Consider that theflip-flop is in active mode. When the input data (D) is applied and when the enable signal (En) is low as in Fig. 4c, the PCLK activates MN5transistor and PCLKB activates MN3. With CLK and CLKB inputs to MN5and MN3respectively, D iscaptured only during a small data pulse window during each rising transition. This does not happen during the fallingtransition. Once the data (D=1) is evaluated, with devices MN4, MN3and MN1 on during the data pulse window, the outputQB becomes Low. It switches the device MP2 on so that Q becomes High. Thus, the data bit applied gets latched to theoutput during the pulse window at the rising edge of the clock. The sinusoidal power clock PCLK shown in Fig.4crecycles the power supply delivered to the node Q, when the power clock is operating in Recovery phase. The lowerpart of the circuit with MN1, MN3and MN4transistors are Offduring the Recovery phase, separating it from the storagenodes Q and QB in the upper half of the circuit. Thus, this arrangement enables better charge recovery avoiding anyinternal redundant switching.

In the progression of the SADGFF flip-flop operation, the following observations can be made:

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1. When the internal clock is blocked, all the internal switching operations are prevented and data also is notconsequently processed. This reduces the clock switching power in the data circuits during the idle mode.
2. Replacing the local inverter with NOR gate reduces the short circuit dissipation due to the increased number ofseries transistors to the ground.

Modeling of the energy recovery property of SADGFF clocked Flip-flop

The time varying clock, when applied as power supply to a conducting MOS device, reduces the potential across its drain and source terminals. This minimizes the channel dissipation in the pull-up and pull-down transistor networks. Furthermore, the energy delivered to the circuit nodes during the Evaluate phase is recycled back to the supply during the Recovery phase. The energy dissipation of the power-clock driven switch, during the evaluating and recovery phases are given by

$$E= (2RonCL / T) Vdd^2 \qquad (1)$$

Here, Ron is the ON resistance of the charging path, CL is the load capacitance of the output node and T is the power clock period. The power-clock is able to recover the nodal charge as long as the amplitude of the power-clock is more than Vth of the device in the recovery path. This contributes to the second term of energy dissipation of Eqn (1). The energy dissipation due to leakage forms the third term of Eqn (2)[8].

$$P=C (Vdd/2)^2 \qquad (2)$$

$$Ci=Cox||Cd||Cif||Cof||Cod \qquad (3)$$

Due to the sinusoidal nature of the clock signal, PCLK is generally less than Vdd/2 for a major portion of the data pulsewindow as shown in Fig. 5. Thus, a larger clocked transistor MN4 can also be used with reduced gate dissipation asshown by

$$Ediss= (2RonCL/T)Vdd^2 +1/2CLVdd^2+Vdd.Ileak.KT(4)$$

Negative setup time

The minimum setup time is the smallest time interval for which the data must remain stable on a data output before it is latched in by an active transition on an appropriate control input. For a D flip-flop, this is the time period for which thedata input D must be maintained, before the arrival of the active level of the clock input.

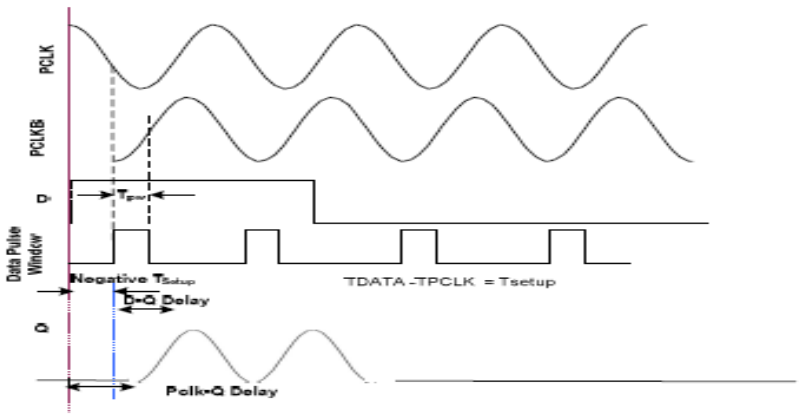

Fig. 5. Timing characteristics of the SADGFF.

The setup time is measuredfrom the clock transition relative to the input data transition at the 50% (default) points as shown in Fig. 5. It is given as Eqn. (5) [9]

$$TD-Q=Tsetup +Tclk(5)$$

Tolerance to Clock Skew and Jitter

This section presents the capability of the proposed design in tolerating the clock skew and jitter. Clock signals aretypically loaded with the larger fan-out, trek over the long interconnect wires, and operate at the highest speeds, withinthe entire synchronous system. Any differences and uncertainty in the arrival times of the clock signals severely limitthe performance of the entire system. It may lead to race circumstances due to which an incorrect data signal may latch within aregister. These uncertainties due

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to the parasitic effects in the clock distribution paths, noise and inaccuracies in theclock generation circuits can produce a temporal or spatial variation in the clock signal resulting in skew and jitter [3].
In this paper, the proposed realizes the following, while operating at a frequency range of 100 to 200 MHz:

1. The negative setup time ensures the signal integrity of the flip-flop
2. It increases the robustness of the design

All the above attributes of the proposed design is appropriately illustrated with the simulation results of the clockdistribution structure presented in the next section.

Clock distribution network with the h-clock tree & 1024 leaf cell

Clock distribution networks synchronize the flow of data among the synchronous data paths. The design ofthese networks can considerably affect the system-wide performance and the reliability. For the analysis of theproposed design, a hierarchical clock tree with the balanced paths along the interconnect lines to each of the leaf cell ischosen for an optimised delay and a minimum skew.

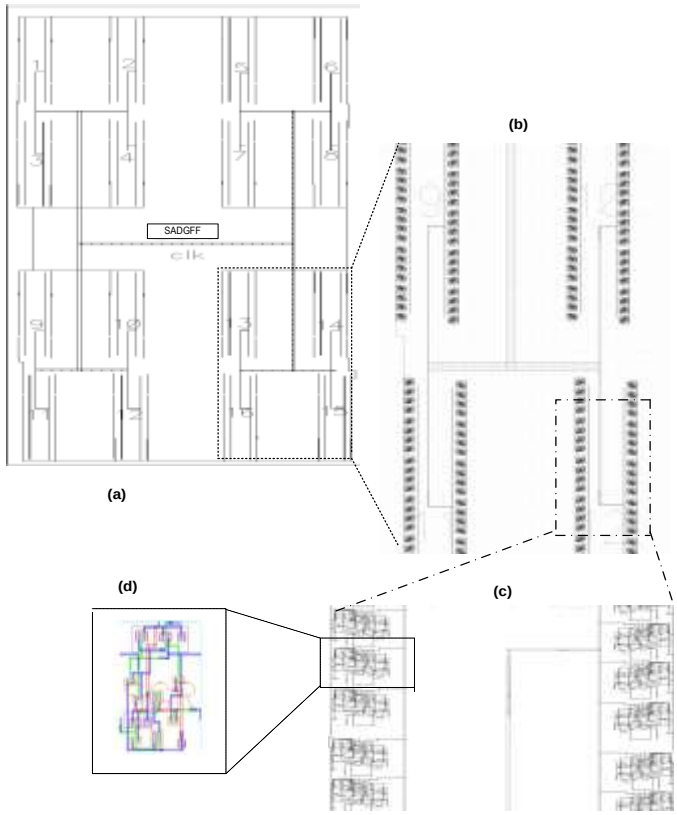

Fig. 6. (a) The full custom overview layout of the SADGFF flip flop with the H-Tree (b) Enlarged view of the leaf cell having branches 13,14,15 and 16,
(c) Enlarged view of the branch 13 with the metals 1 to 6 at the H-tree leaf and (d) The layout view of the single SADGFF clocked flip-flop.

The H-clock tree is unbuffered and is driven by a resonant clock. It has 16 clock nodes with two 32 bitregisters at each of its clock nodes, i.e., 1024 leaf cells. These leaf cells are replaced one by one with the SAER, SDER and SADGFF flip-flops for simulation and justifiable comparison for their power and timing parameters. The full customised layout representation of the clock distribution structure with the enlarged views of the hierarchy of modular components is presented in Fig. 6(a), 6(b), 6(c) and 6(d). Further, the decreased device dimensions due to technology scaling has increased the global interconnect line resistance and has particularly affected the clock signal distribution issues. The increased line resistance is one of the major factors, which imparts the growing importance of the clock distribution on the synchronous system performance.
In this paper, the metal 4 layer is chosen for designing the H-clock tree with the minimum line resistance. And also, any differences in the delay of the clock signals can severely limit the maximum frequency performance of the entire system. It may, in addition, create the catastrophic *race* conditions [7], in which an incorrect data signal may latch within aregister. Thus, the full customized balanced path design of the H-clock distribution network, as employed in this work, further ensures that these critical timing requirements are satisfied and that the correct data is latched to the output.

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Simulation results and analytical justification

The schematic design and the layout simulations have been carried out using the 45nm process technologylibraries, employing the Cadence® Spectre and Assura tools. The simulations are done using the power clock of peakvoltage 1.1V operating at the frequency range of 100-200MHz. For justifiable comparisons, the simulation is done forall the existing flip-flop architectures and the proposed SADGFFflip-flop. The simulation test bench is the customdesignedH-clock tree driving two numbers of 32-bit registers, thus driving 1024 leaf cells.

The simulation results prove that the proposed flip-flop structure is dissipating less dynamic power than theexisting energy recovery flip-flops, which are powered by a constant supply voltage *Vdd.* The power dissipation in thestorage nodes of such flip-flops are given by Eqn. (6).

$$PD = \alpha C_L V_{DD}^2 f \quad (6)$$

Here, $V_{DD}$is the supply voltage, f is the operating frequency, $C_L$is the load capacitance and the switching activity factor$\alpha = 1$[1].

The results shown in Fig. 7(a).depict the fact that the decreased numbers of transistors result in reduced CL contributing to an enhanced switching power efficiency of the

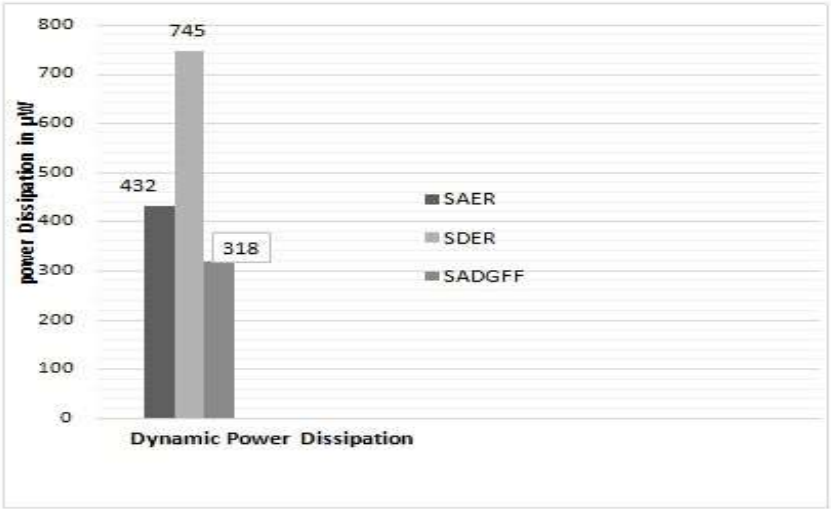

Fig. 7(a). Comparison of the dynamic power dissipation.

proposed flip-flop structure. For justifiable comparisons,the simulations have been done for all the existing flip-flop architectures in the literature and the proposed SADGFF clockedflip-flop. The simulation results show that the dynamic power dissipation of the SADGFF clocked flip-flop design is324nW.

Thus, it is 26% and 56% more power efficient than the SAER (439 nW) and SDER (753 nW) flip-flops, respectively.

Fig. 7(b). Power dissipation PD at various Switching activity.

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Table.1
Comparison of the power dissipation results at 200 mhz frequency of operation and 100% data switching rate

Flip Flop	Clock Power in µW	Flip flop Power dissipation in µW	Total Power dissipation in µW
SAER	5.78	432.1	452.9
SDER	2.712	745.2	754.12
SADGFF	21.72	318.05	343.53

For a comprehensive analysis, the dynamic power dissipation of the SADGFF clocked flip-flop is measured fordifferent switching activities, at the maximum operating frequency of 200MHz. The proposed flip-flop is proved to bemore power efficient the various switching data rates also, while comparing with the existing energy recovery flip-flopsin the literature. The results are plotted in Fig. 7(b).
Further, the dynamic dissipation of all the 1024 flip-flops summed up for each type along with their correspondingclock tree power dissipation are shown in Table I. The minimized nodal clock capacitance as identified in Eqn. (4)contributes to the energy reduction of the proposed SADGFF clocked flip-flop. The leakage current is also reduced in theproposed structure due to the advantage of the stacked transistors *MN1*, *MN2*, *MN3*and *MN4*. The simulation results show thatthe leakage power dissipation of the proposed design SADGFF is 78% less than SDER.

Table2
Comparison of te timing parameters at 200mhz frequency of operation and 100% data switching rate

Type of flip flop	Setup time in ns	Hold time in ns	D-Q delay in ns	Clk-Q delay in ns
SAER	10.366	4.005	15.71	5.55
SDER	6.011	1.39	14.01	8.71
SADGFF	1.27	4.6	10.2	9.91

Moreover, the SADGFF Flip-Flop realizes the setup time of Tsetup = -1.27ns. This negative setup time Tsetup presentsthe reduced D-Q delay of 10.2ns as per the Eqn. (5).thus improving the timing performance of the flip-flop. The timingparameters are tabulated in Table II for all the energy recovery flip-flops at 200 MHz frequency of operation and 100%data switching rate. As observed from the table, negative set up time improves the signal integrity of the proposedstructure, ensuring that the design can endure clock skew and jitter to a greater extent than its counterparts.

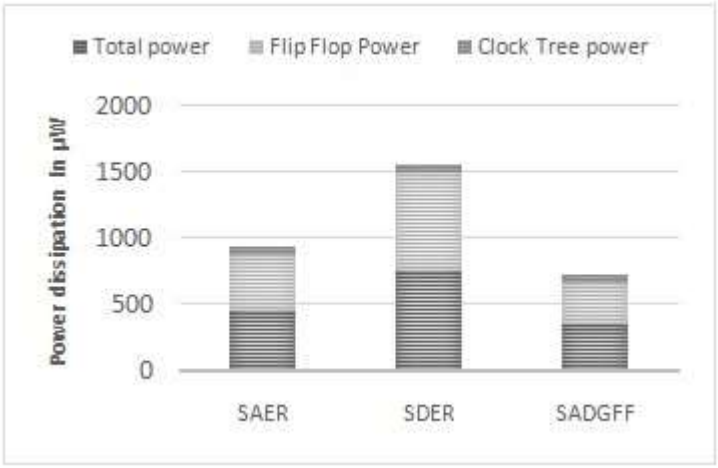

Fig. 8(a). Comparisons of the energy savings.

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The flip-flop power dissipation and total power dissipation efficiency of the self-gated differential clocked flip-flopover the other flip-flops are depicted in Fig. 8(a). The total power dissipation of the 1024 flip-flops of the SADGFF(343.7μW) is found to be 25% and 56% power efficient than the SDER and SAER respectively.
The proposed flip-flop structure is also analysed for both the sleep mode and active mode of operation. Fig. 8(b).depicts the

Fig. 8(b). Sleep mode Power dissipation with and without Clock Gating.

power dissipation values incurred in the sleep mode with and without clock gating for the proposed flip-flop. The result indicates that the proposed flip-flop is dissipating 325.69 μW power in the sleep mode with α=1switching activity without clock gating. The same setup with the differential gating structure dissipates 323.53 μW of power.
The resulting 6% reduced power dissipation is due to differential gating structure introduced in the SADGFF clocked flip-flop.From the simulation results and discussions, it is apparent that the Sense Amplified Differential Gated (SADGFF) clocked flip-flop designpresented in the paper mitigates most of the prevalent issues found in the energy recovery clocked flip-flopcounterparts. Besides, it specifically addresses and optimizes the flip-flop power dissipation which is the majorcontributor to the total power dissipation

Conclusion

This paper proposes a novel SADGFF clocked flip-flop, which achieves a negative setup time of 1.27ns, aminimum hold time of 4.6ns and the least D-Q delay of 10.2nnns. The results validate its improved performance andtiming attributes. Further, the proposed SADGFF structure is found to dissipate a reduced dynamic power dissipation of324nW, when compared with the existing flip-flop architectures, namely, SAER and SDER. This paper also illustratesthe power benefits of the proposed structure in comparison against the existing architectures, for different rates ofswitching activity. The total power dissipation efficiency of the 1024 flip-flops structure using the SADGFF (measured as343.53μW) is found to be 25% and 56% better than the SDER and SAER counterparts, respectively. And furthermore,the SADGFF clocked flip-flop is proved to possess an inherent robustness to the clock skew and jitter due to its negativesetup time, achieved by the circuit and is hence found more suitable for the local clock grid distribution structures thatmay incur the maximum skew. Thus, the proposed low power clocked flip-flop structure can contribute to theminimization of clock power dissipation, dynamic power dissipation and the leakage power dissipation, making it idealfor hierarchical clock tree distribution that may have maximum dissipation. Additionally, the circuit is found to realizeenhanced performance, and is suitable for both the critical and non-critical paths.

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INTERNATIONAL JOURNAL OF RESEARCH SCIENCE & MANAGEMENT

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